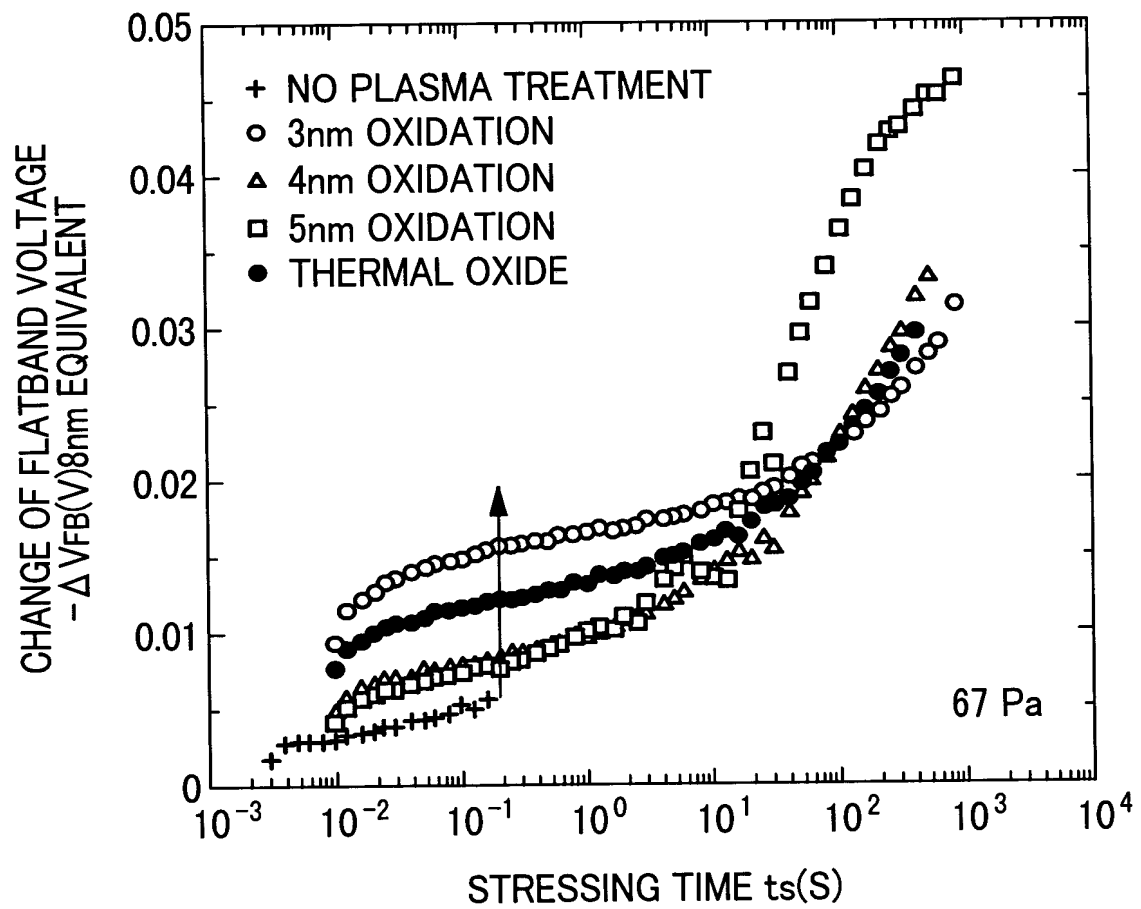


FIG.1



# FIG.2

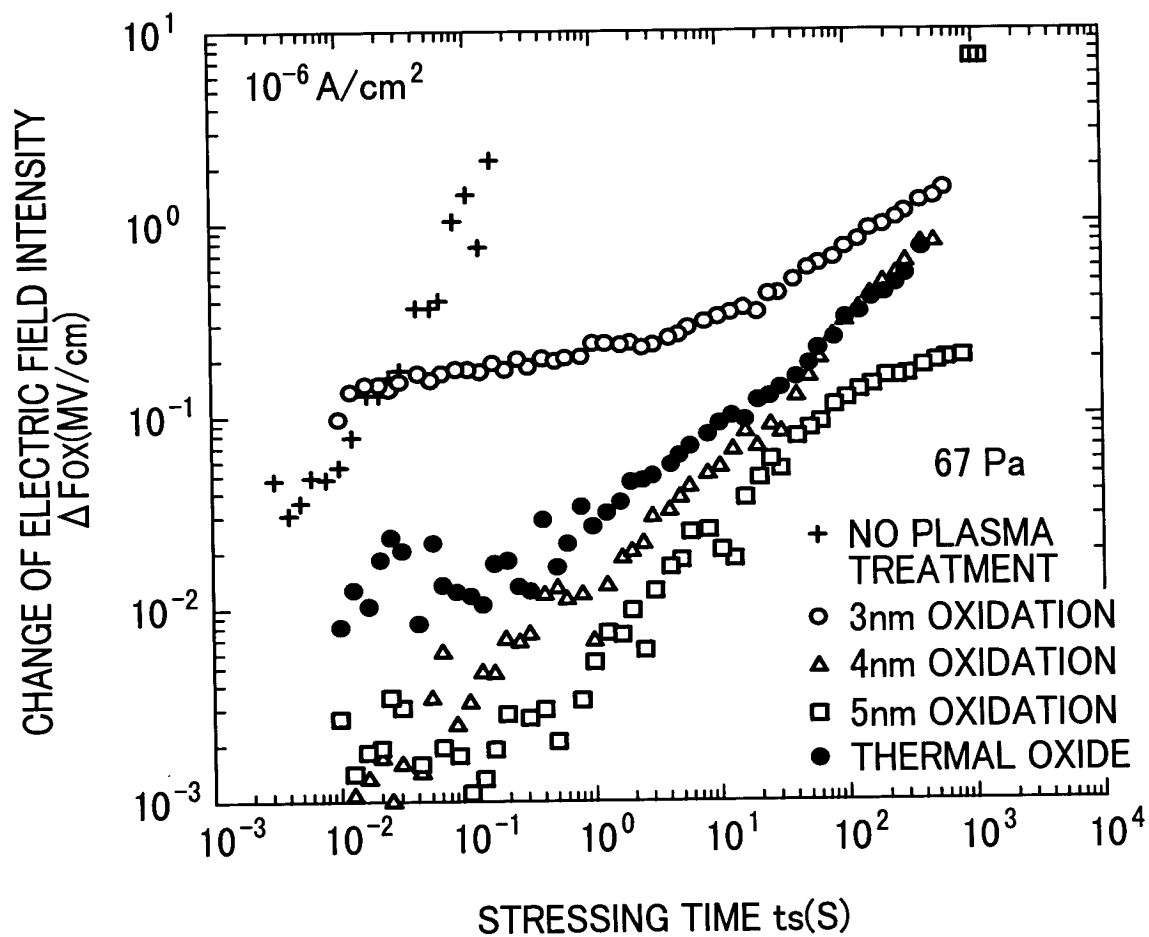


FIG.3

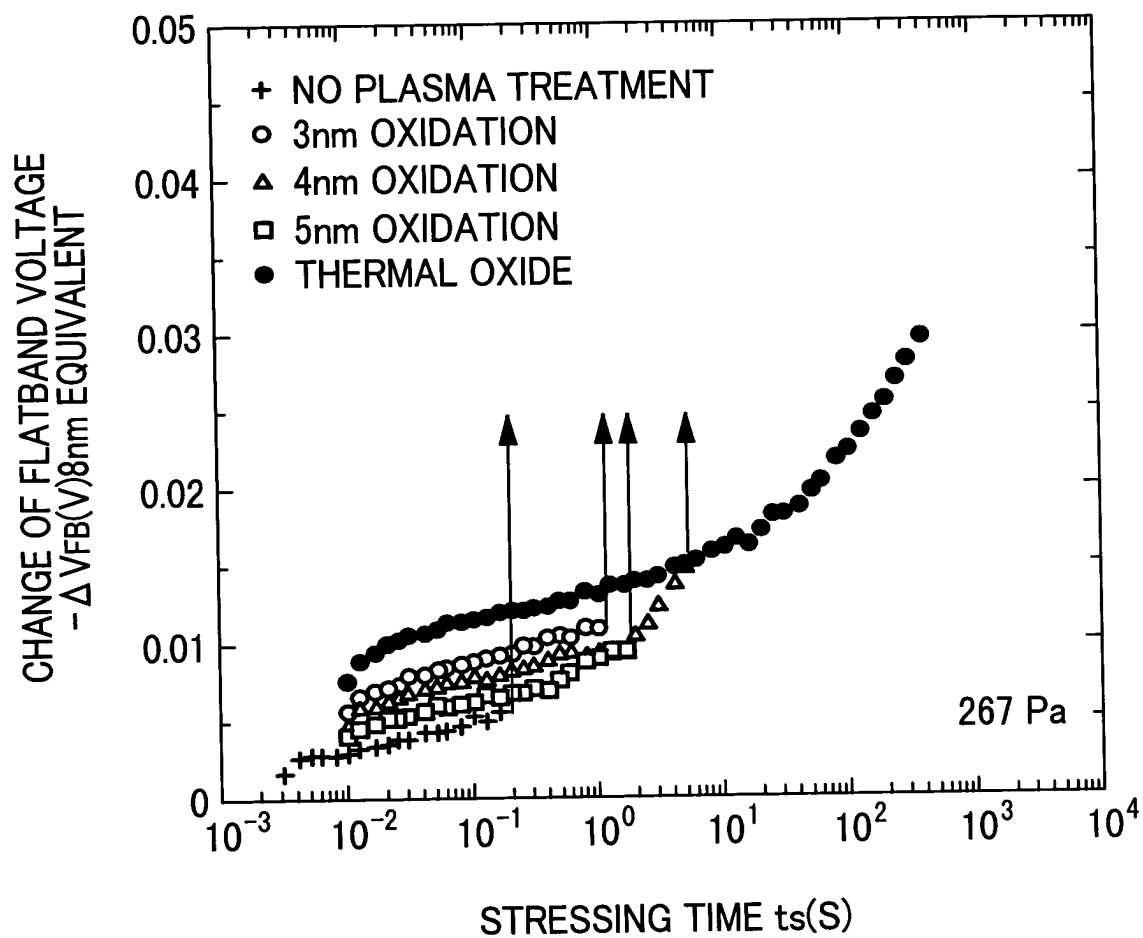


FIG.4

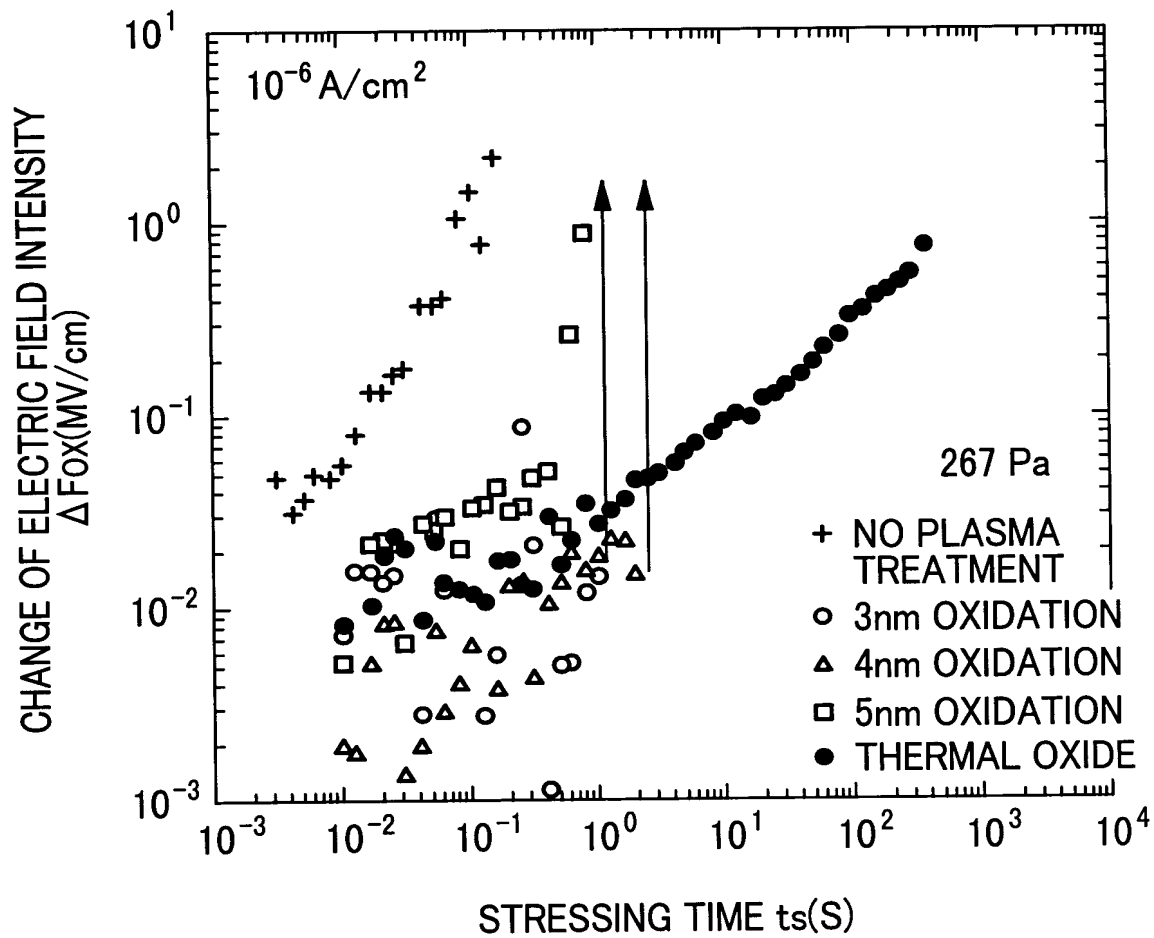


FIG.5

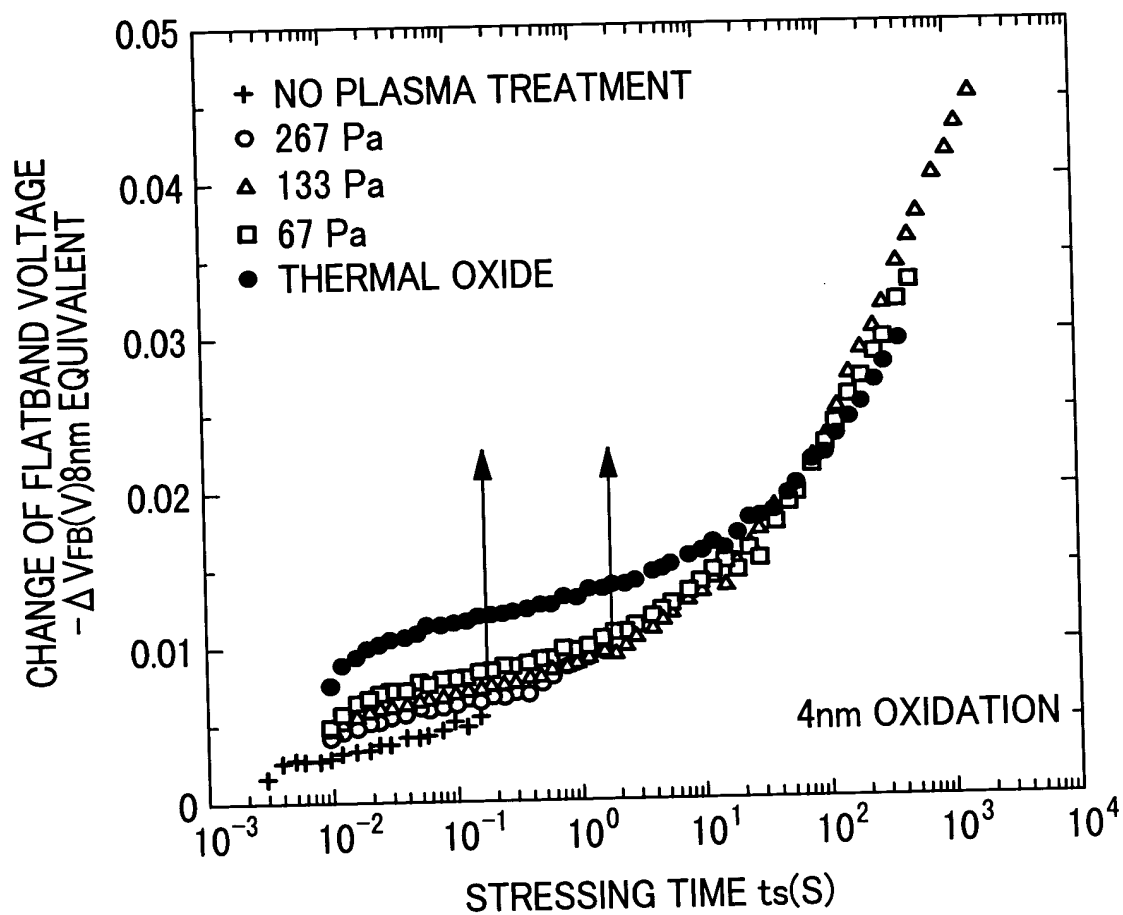


FIG.6

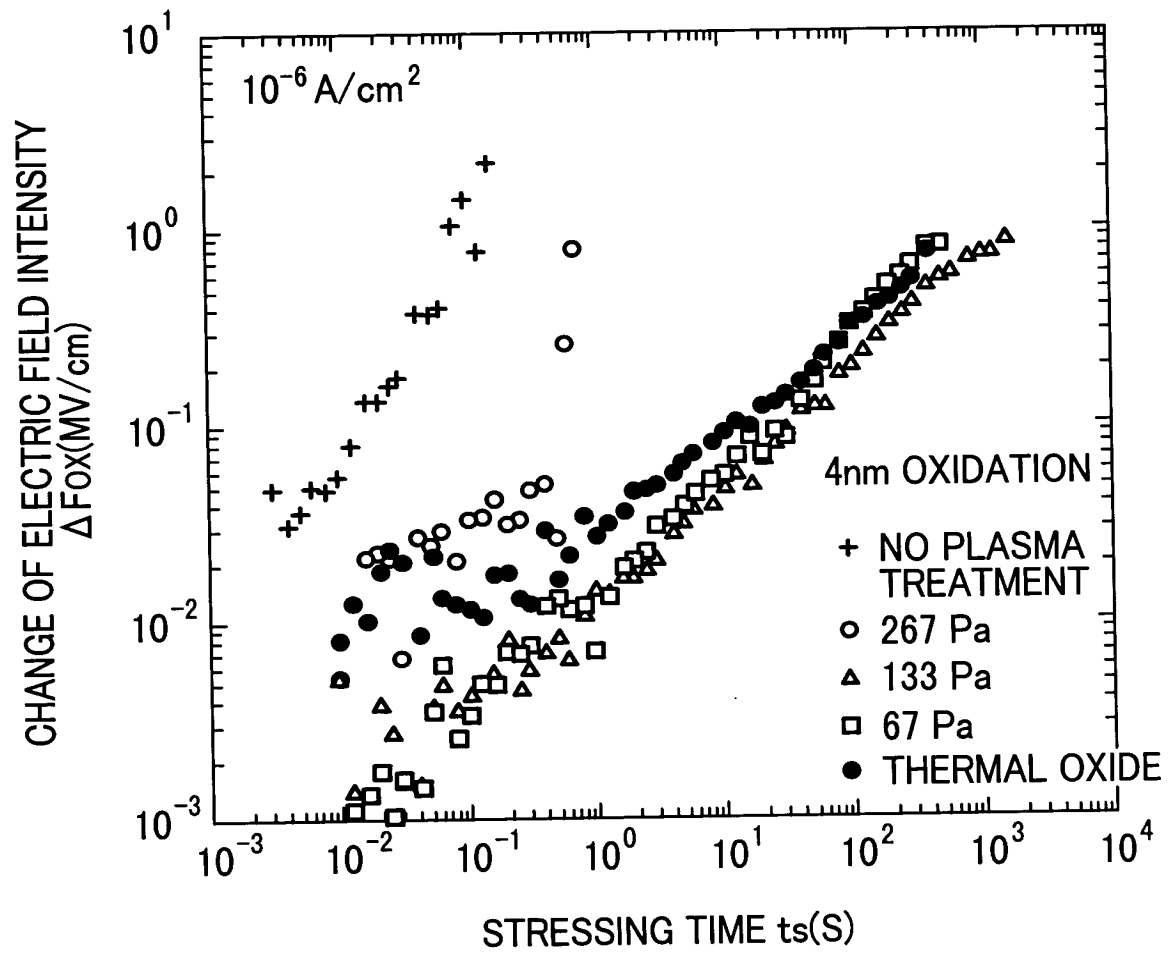
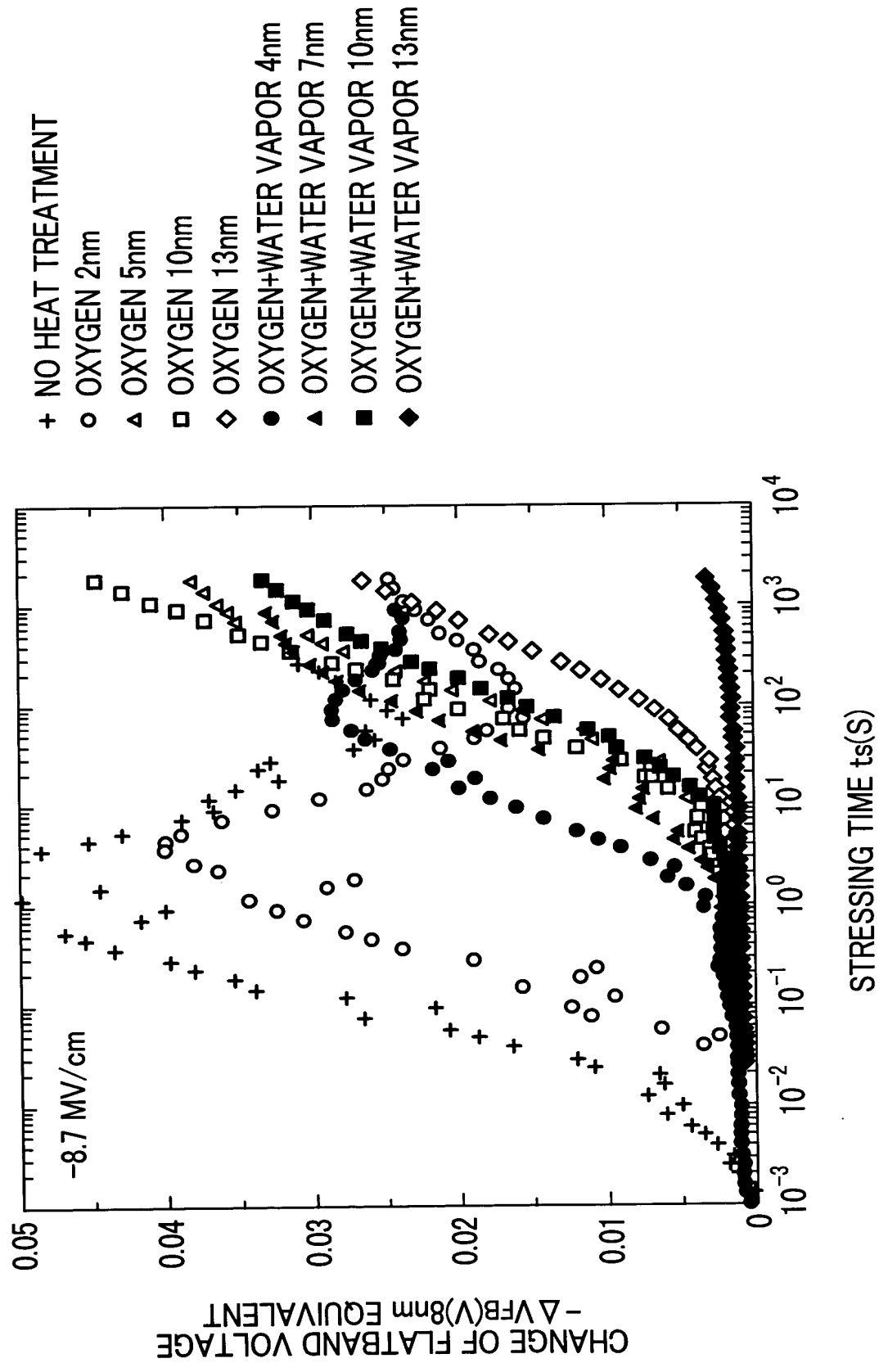
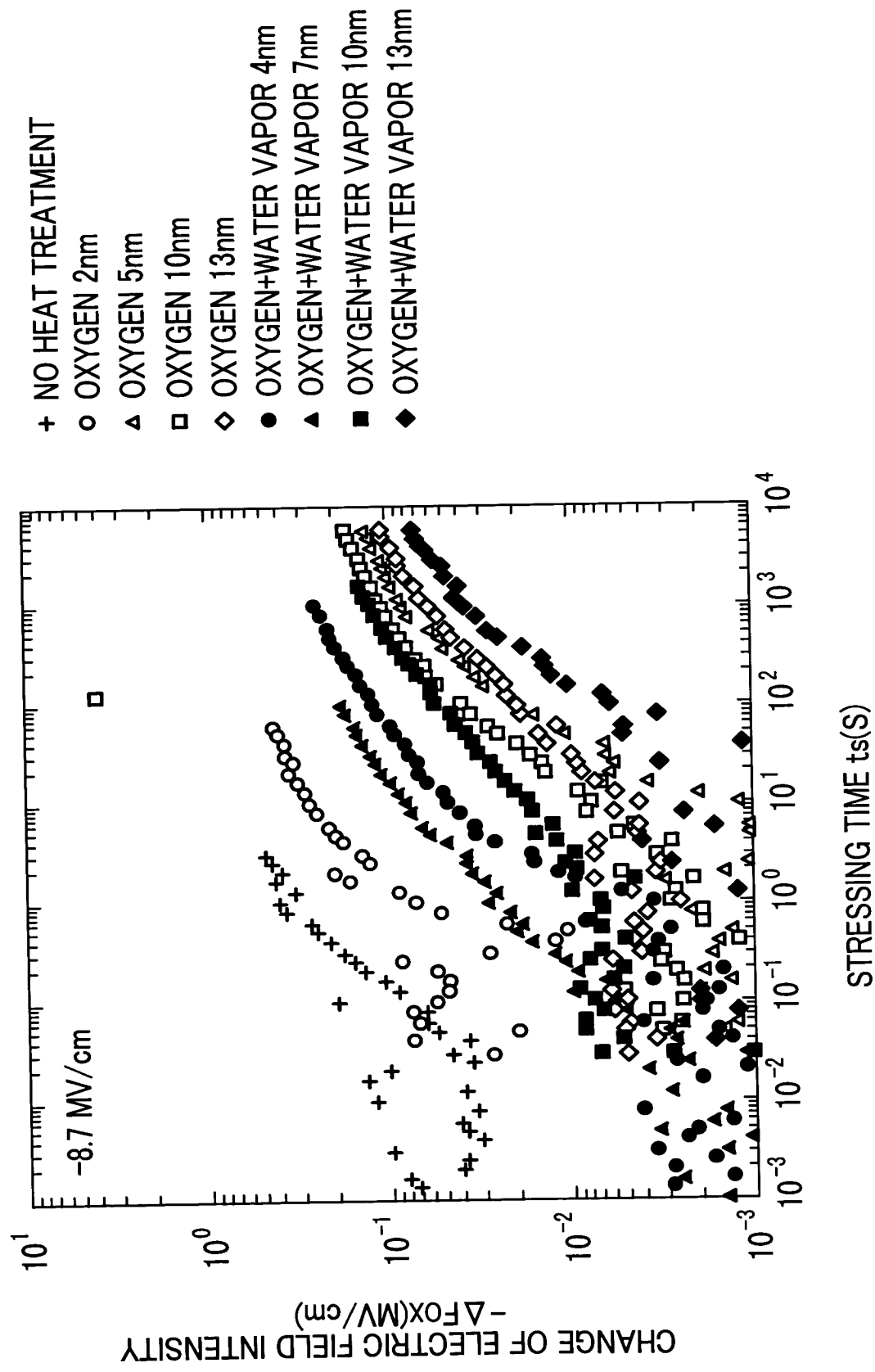


FIG.7

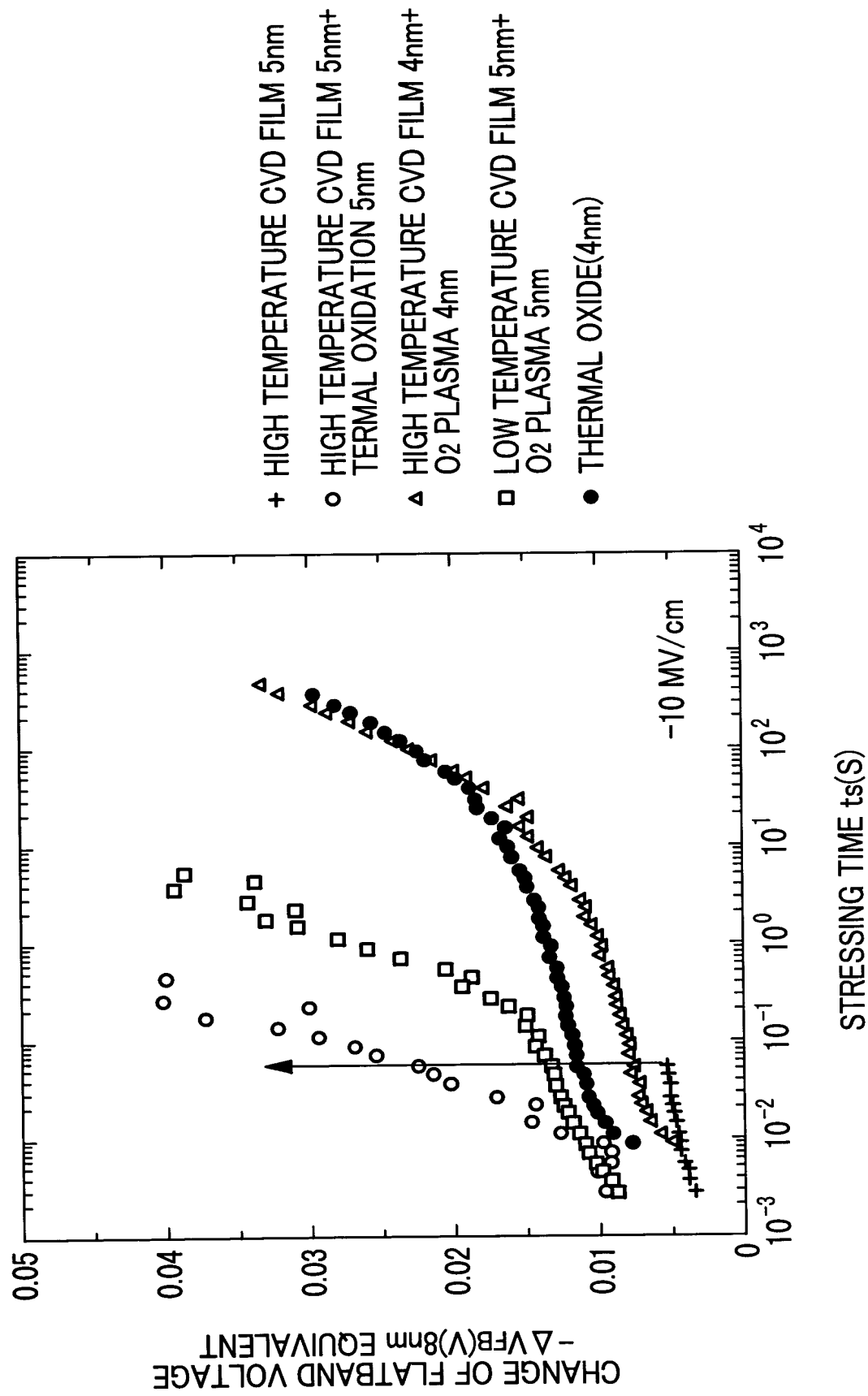


# FIG.8





# FIG.9



# FIG.10

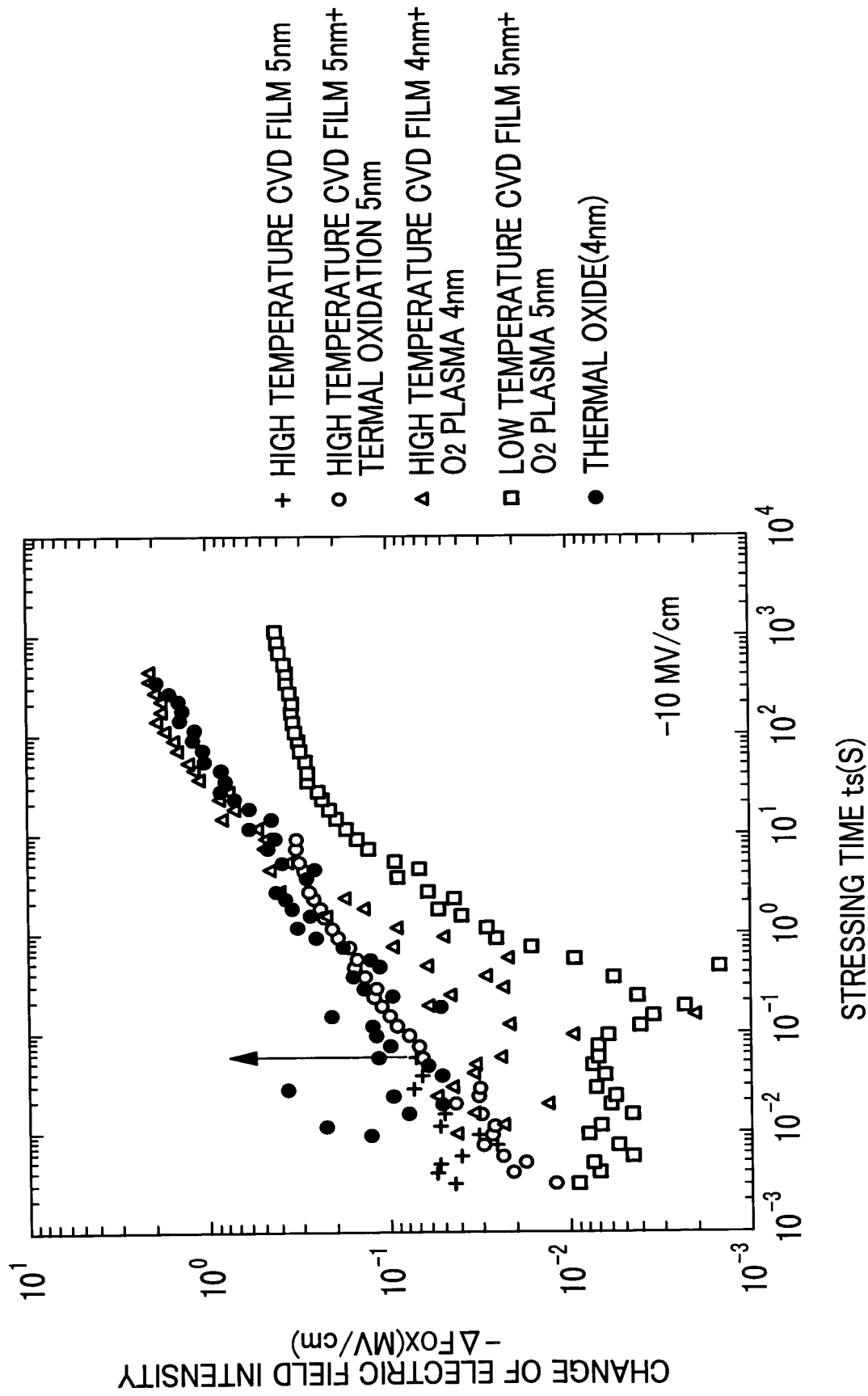


FIG.11

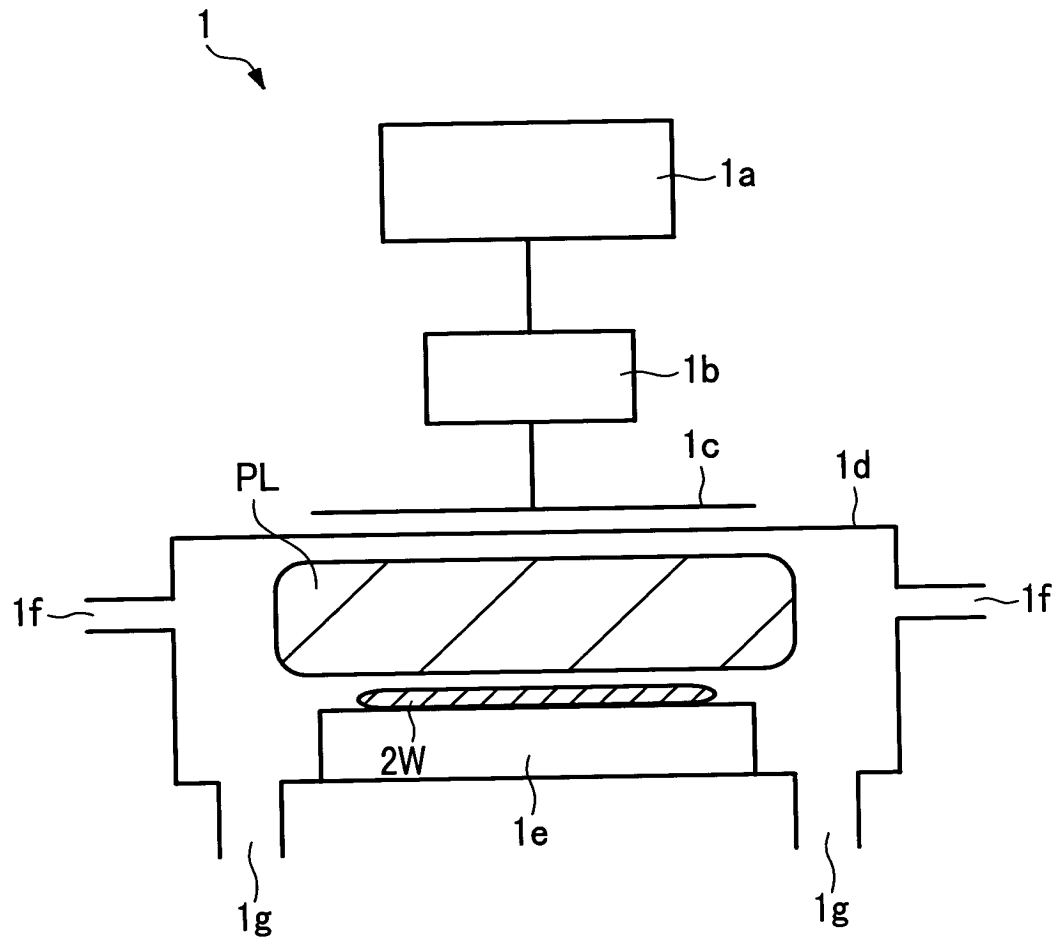
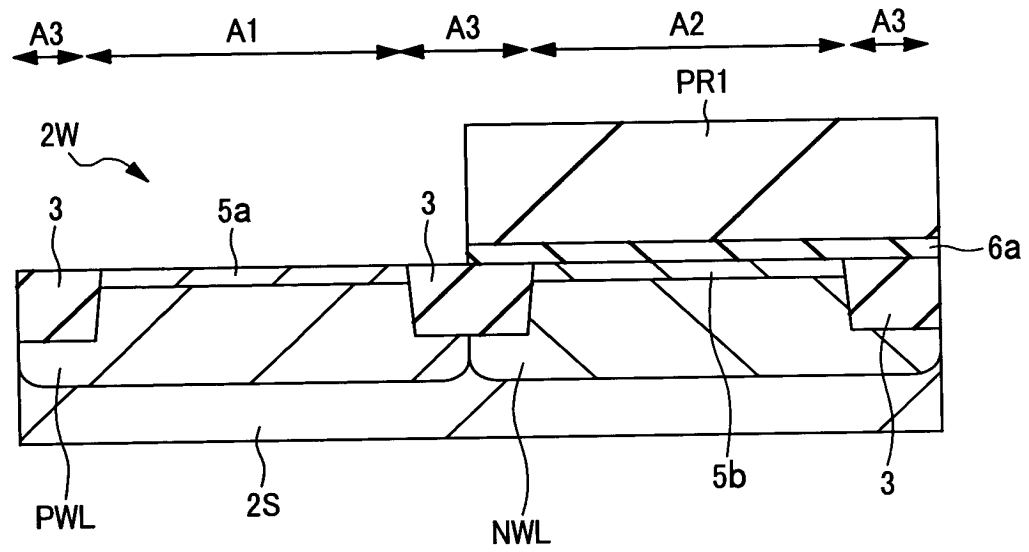
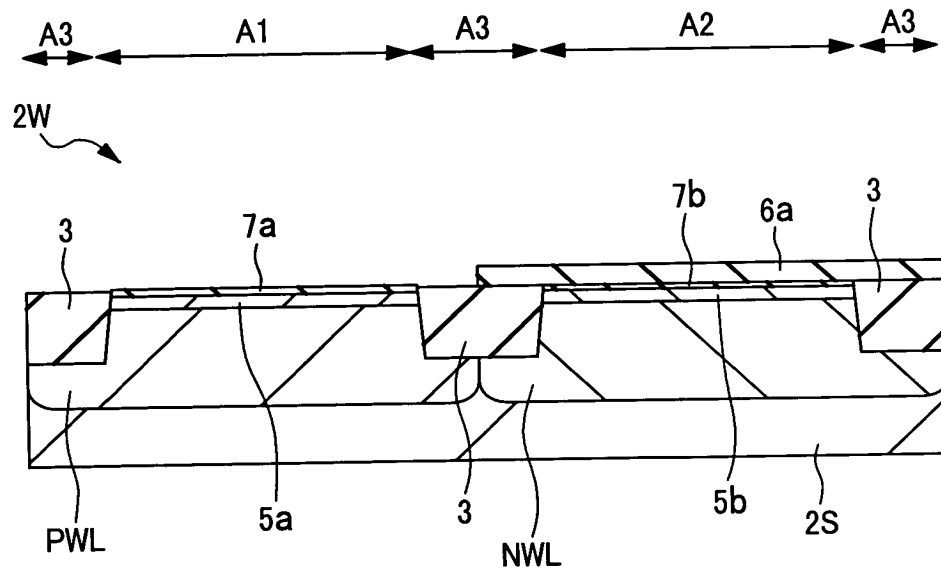


Figure 1 consists of two parts: a plan view (top) and a cross-sectional view (bottom). The plan view shows a series of rectangular regions labeled A1, A2, and A3, with arrows indicating a direction. The cross-sectional view shows a layered structure with labels 3, 4, 5a, 5b, 2S, PWL, and NWL. A dimension 2W is indicated for the width of the structure.

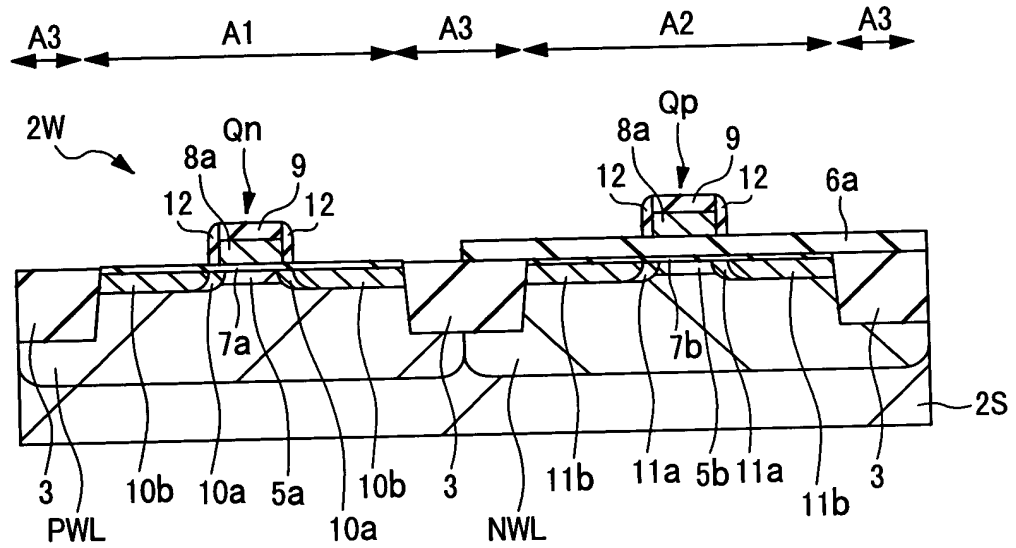
# FIG.14



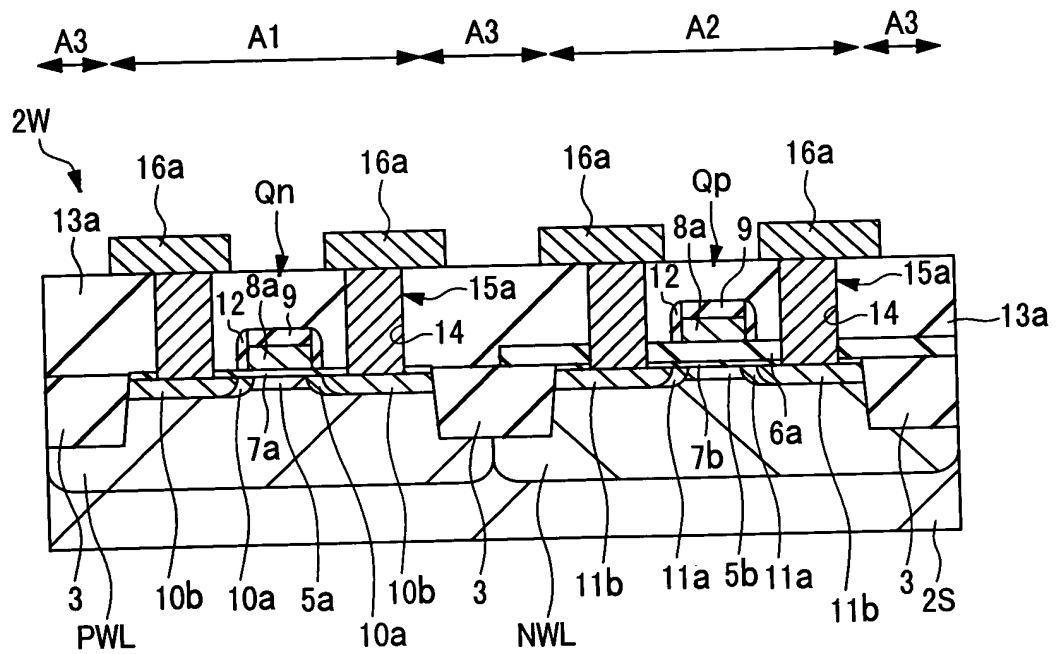
# FIG.15



# FIG.16

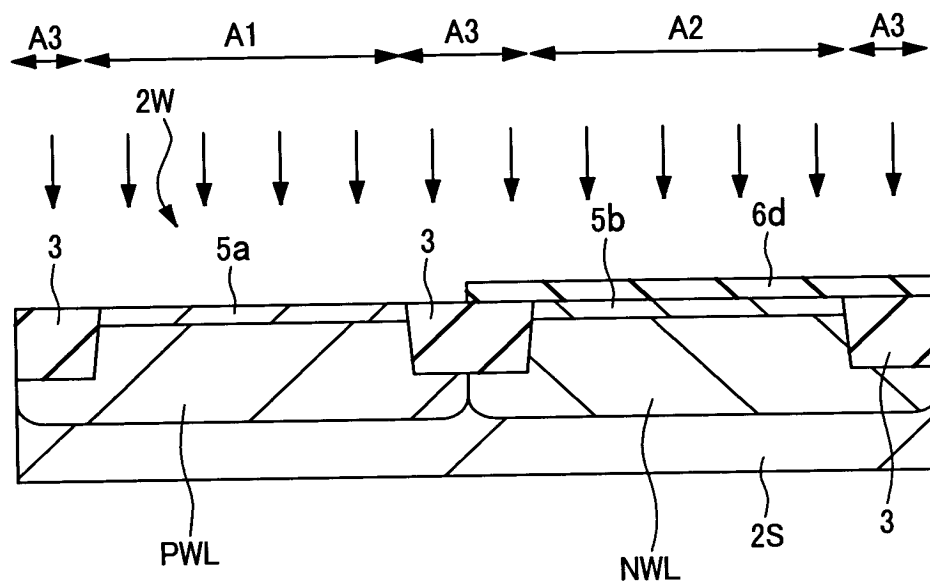


# FIG.17

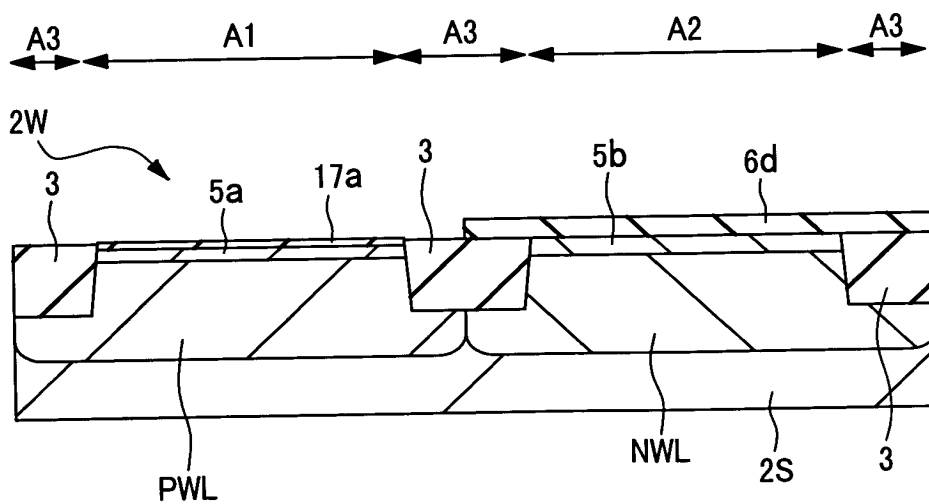


This diagram shows a cross-sectional view of a semiconductor device. The structure consists of several layers: a top layer (3), a patterned layer (PWL), a middle layer (5a), another patterned layer (NWL), a bottom layer (5b), and a substrate (2S). The device features a central raised region (6b) and side regions (6c). A series of downward arrows labeled '2W' indicate a uniform load or pressure applied across the top surface. Above the device, a horizontal line with arrows at both ends is divided into segments labeled A1, A3, A2, and A3, likely representing different material regions or measurement points.

# FIG.20



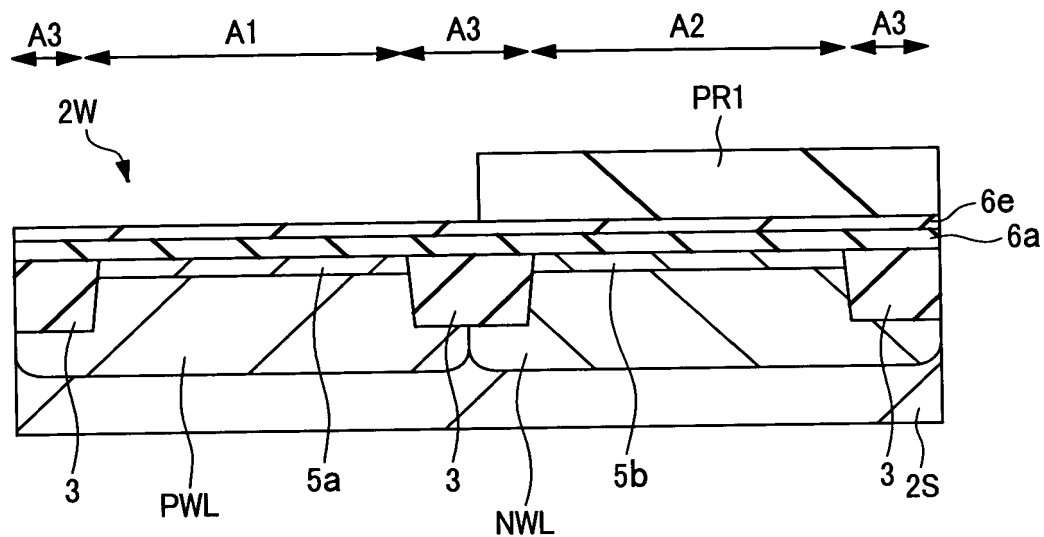
# FIG.21







# FIG.23



# FIG.24

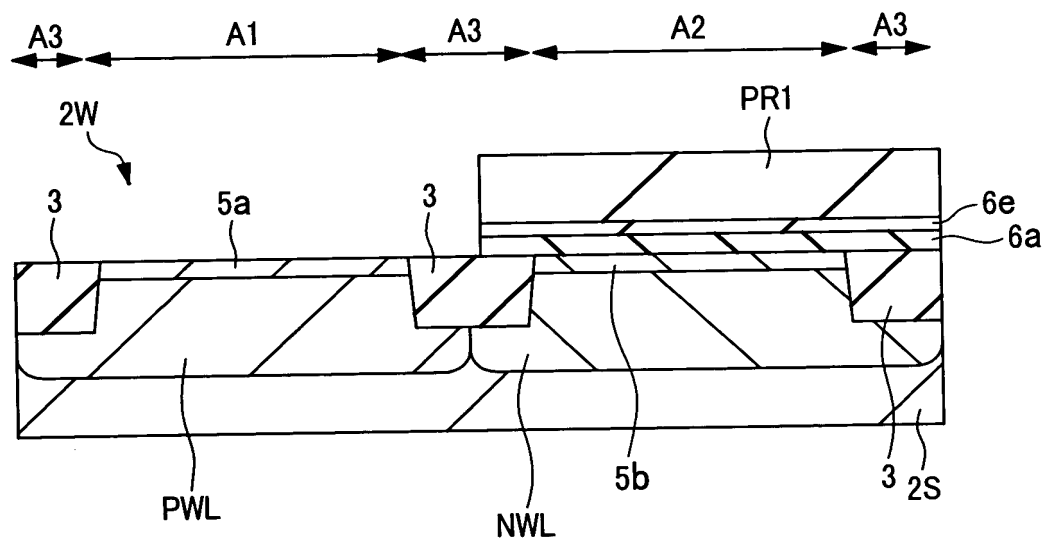


Figure 1 consists of two parts: a plan view (top) and a cross-sectional view (bottom). The plan view shows a series of rectangular regions labeled A1, A2, and A3, with dimensions 2W and 2S indicated. The cross-sectional view shows the device structure with layers labeled PWL, NWL, 3, 5a, 5b, and 6a.

A cross-sectional view of a semiconductor device. The device features a substrate with a patterned gate structure. The gate structure consists of a series of rectangular segments (3) separated by narrow gaps (5a, 5b). The segments are connected to a common gate line (6a). The device is divided into regions A1, A2, and A3, which are separated by narrow gaps (A3). The width of the device is indicated as 2W. The device is labeled with various components: 3 (gate segments), 5a, 5b (gaps), 6a (gate line), 7a, 7b (insulating layers), 8a, 8b (contact layers), 9a, 9b (source/drain regions), 10a, 10b (gate regions), 11a, 11b (gate regions), 12a, 12b (gate regions), 13a, 13b (gate regions), 14a, 14b (gate regions), 15a, 15b (gate regions), 16a, 16b (gate regions), 17a, 17b (gate regions), 18a, 18b (gate regions), 19a, 19b (gate regions), 20a, 20b (gate regions), 21a, 21b (gate regions), 22a, 22b (gate regions), 23a, 23b (gate regions), 24a, 24b (gate regions), 25a, 25b (gate regions), 26a, 26b (gate regions), 27a, 27b (gate regions), 28a, 28b (gate regions), 29a, 29b (gate regions), 30a, 30b (gate regions), 31a, 31b (gate regions), 32a, 32b (gate regions), 33a, 33b (gate regions), 34a, 34b (gate regions), 35a, 35b (gate regions), 36a, 36b (gate regions), 37a, 37b (gate regions), 38a, 38b (gate regions), 39a, 39b (gate regions), 40a, 40b (gate regions), 41a, 41b (gate regions), 42a, 42b (gate regions), 43a, 43b (gate regions), 44a, 44b (gate regions), 45a, 45b (gate regions), 46a, 46b (gate regions), 47a, 47b (gate regions), 48a, 48b (gate regions), 49a, 49b (gate regions), 50a, 50b (gate regions), 51a, 51b (gate regions), 52a, 52b (gate regions), 53a, 53b (gate regions), 54a, 54b (gate regions), 55a, 55b (gate regions), 56a, 56b (gate regions), 57a, 57b (gate regions), 58a, 58b (gate regions), 59a, 59b (gate regions), 60a, 60b (gate regions), 61a, 61b (gate regions), 62a, 62b (gate regions), 63a, 63b (gate regions), 64a, 64b (gate regions), 65a, 65b (gate regions), 66a, 66b (gate regions), 67a, 67b (gate regions), 68a, 68b (gate regions), 69a, 69b (gate regions), 70a, 70b (gate regions), 71a, 71b (gate regions), 72a, 72b (gate regions), 73a, 73b (gate regions), 74a, 74b (gate regions), 75a, 75b (gate regions), 76a, 76b (gate regions), 77a, 77b (gate regions), 78a, 78b (gate regions), 79a, 79b (gate regions), 80a, 80b (gate regions), 81a, 81b (gate regions), 82a, 82b (gate regions), 83a, 83b (gate regions), 84a, 84b (gate regions), 85a, 85b (gate regions), 86a, 86b (gate regions), 87a, 87b (gate regions), 88a, 88b (gate regions), 89a, 89b (gate regions), 90a, 90b (gate regions), 91a, 91b (gate regions), 92a, 92b (gate regions), 93a, 93b (gate regions), 94a, 94b (gate regions), 95a, 95b (gate regions), 96a, 96b (gate regions), 97a, 97b (gate regions), 98a, 98b (gate regions), 99a, 99b (gate regions), 100a, 100b (gate regions).

FIG.27

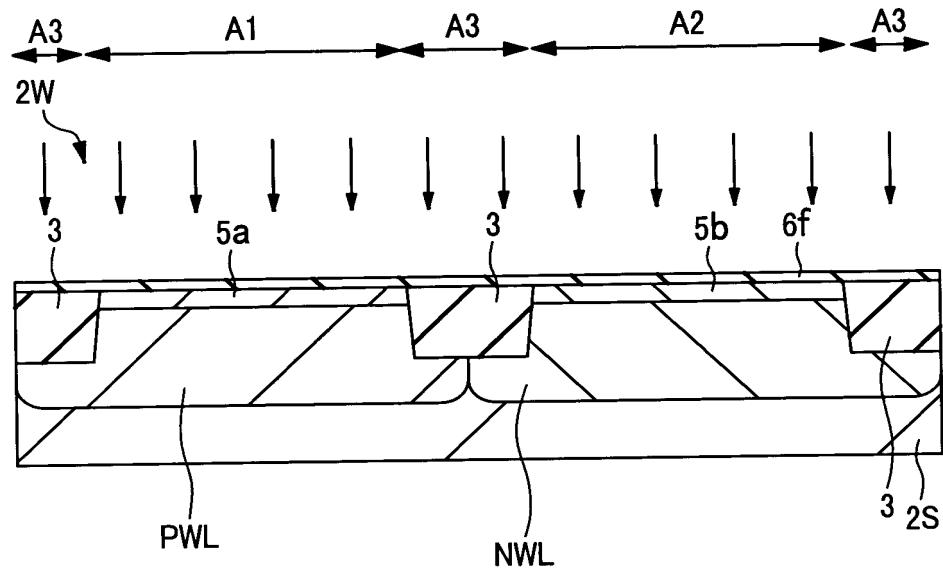
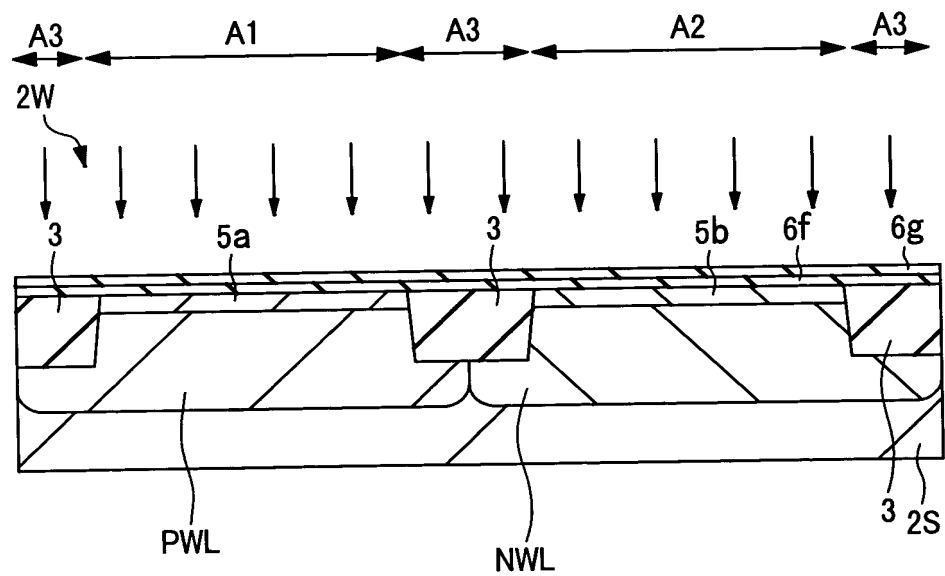
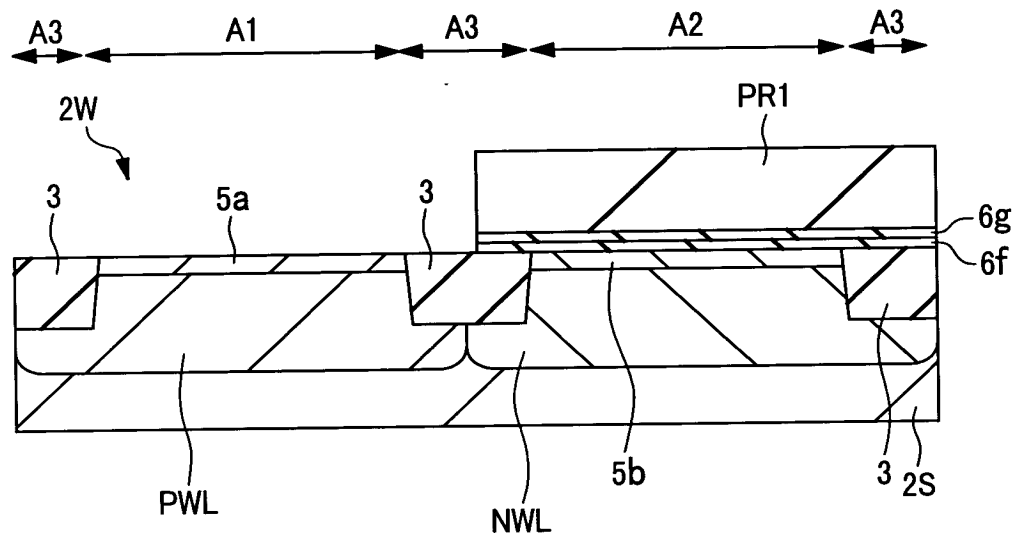


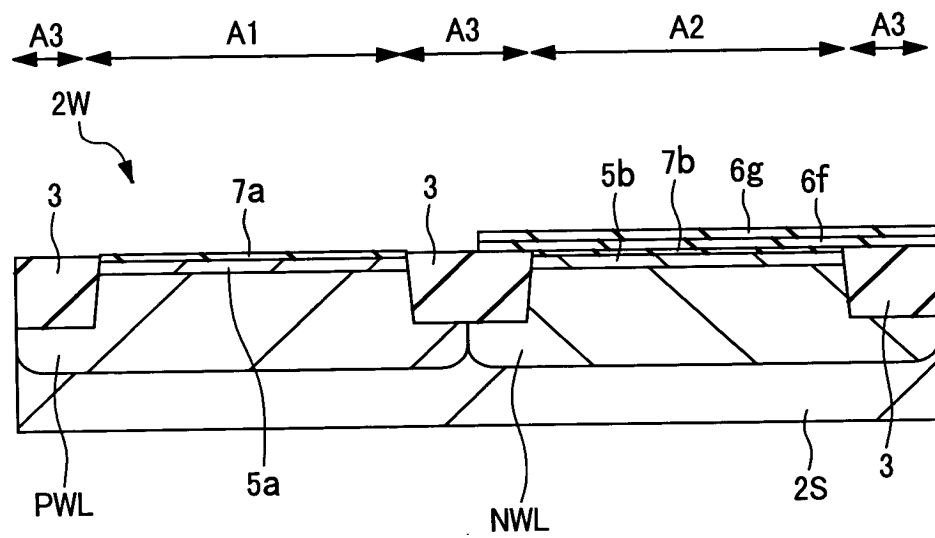
FIG.28



# FIG.29

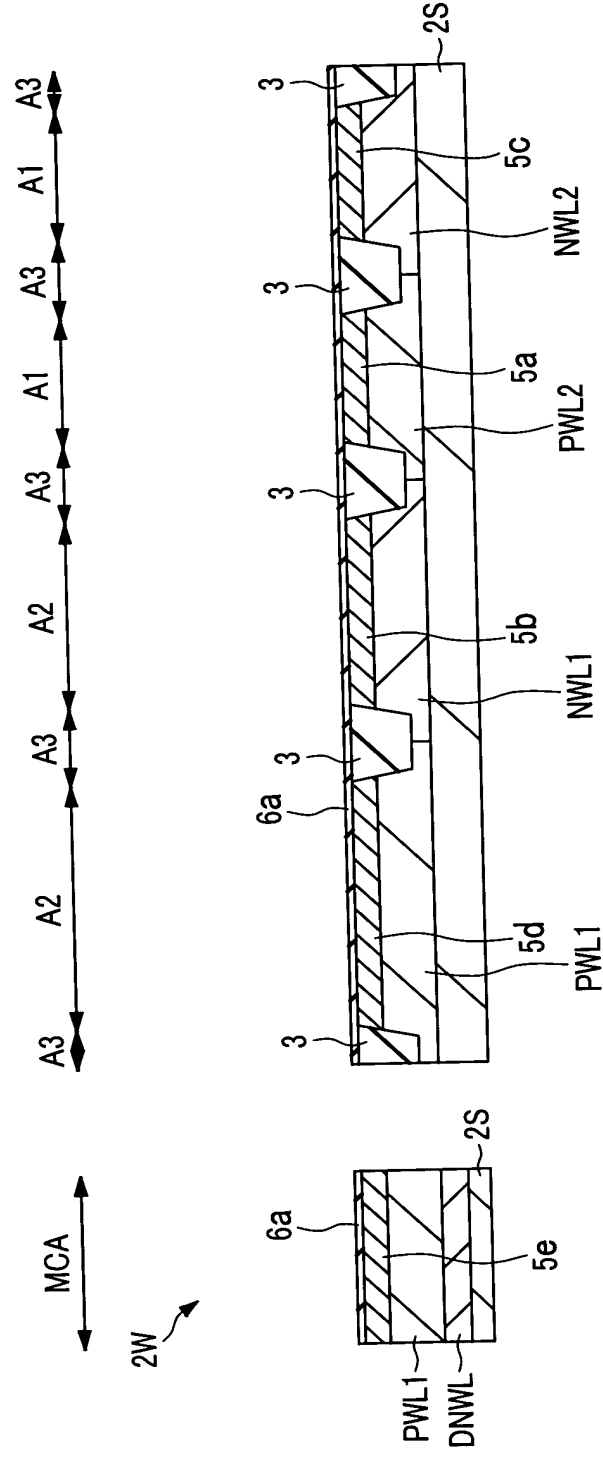


# FIG.30

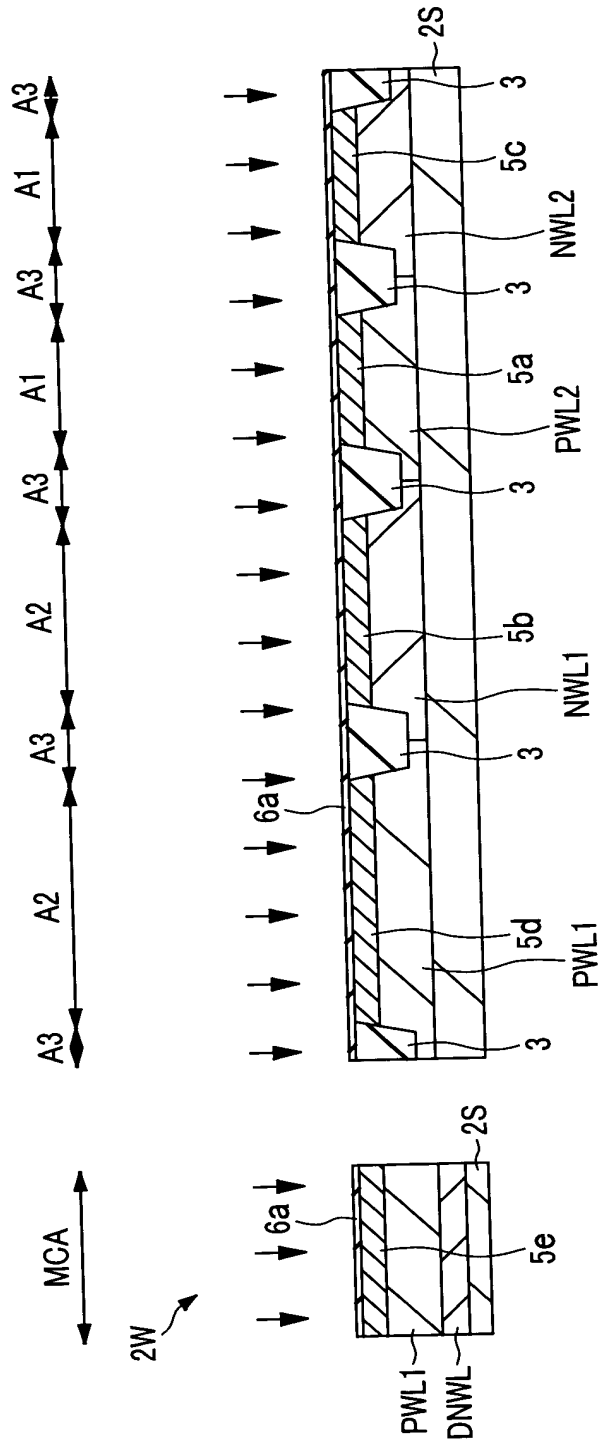


[illegible]

# FIG.32

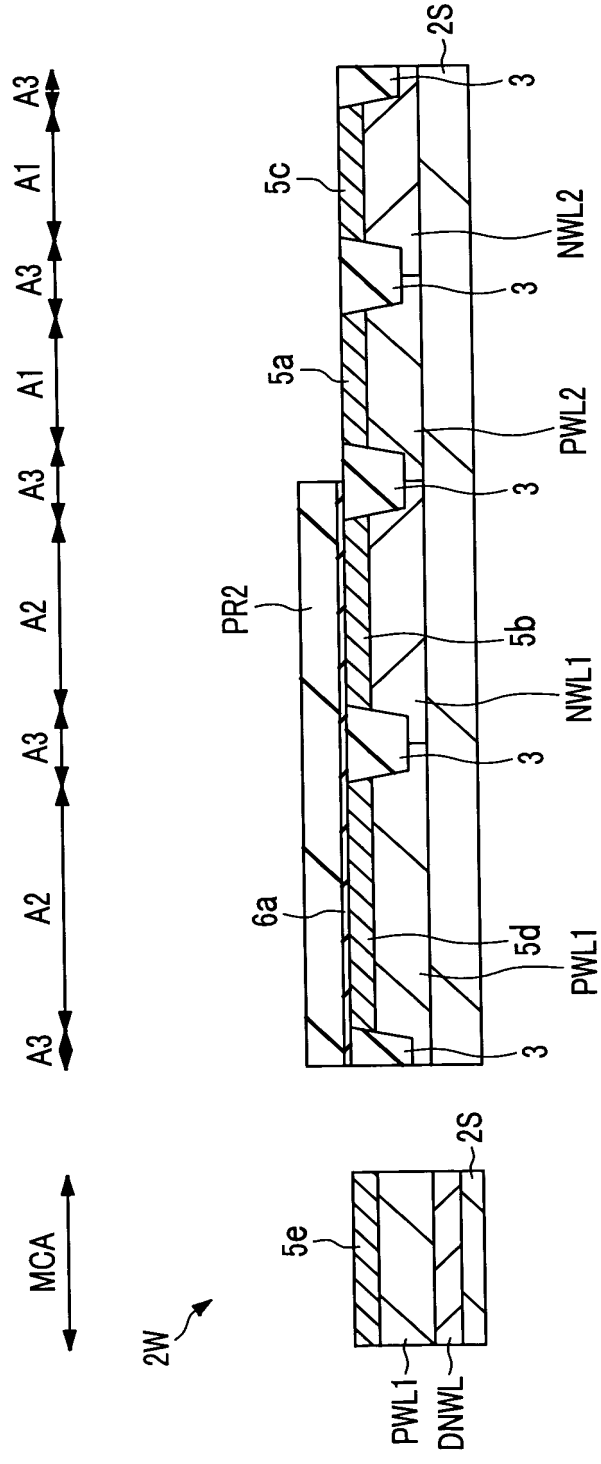


# FIG.33

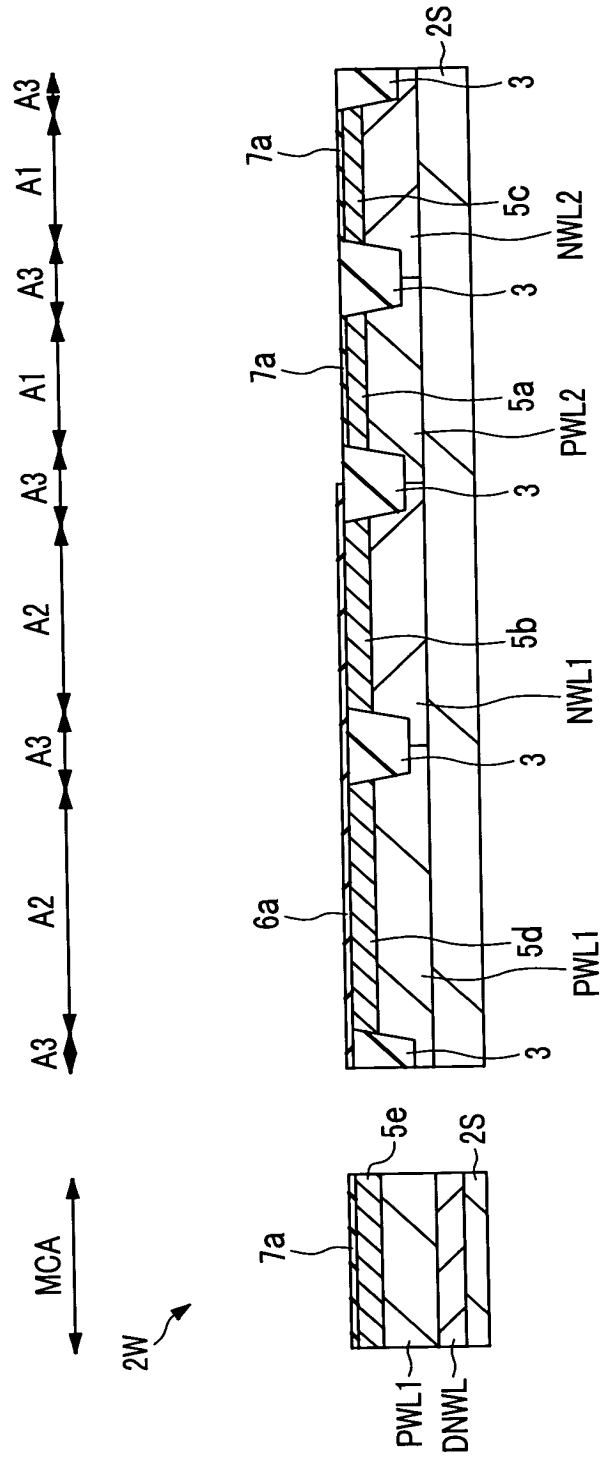




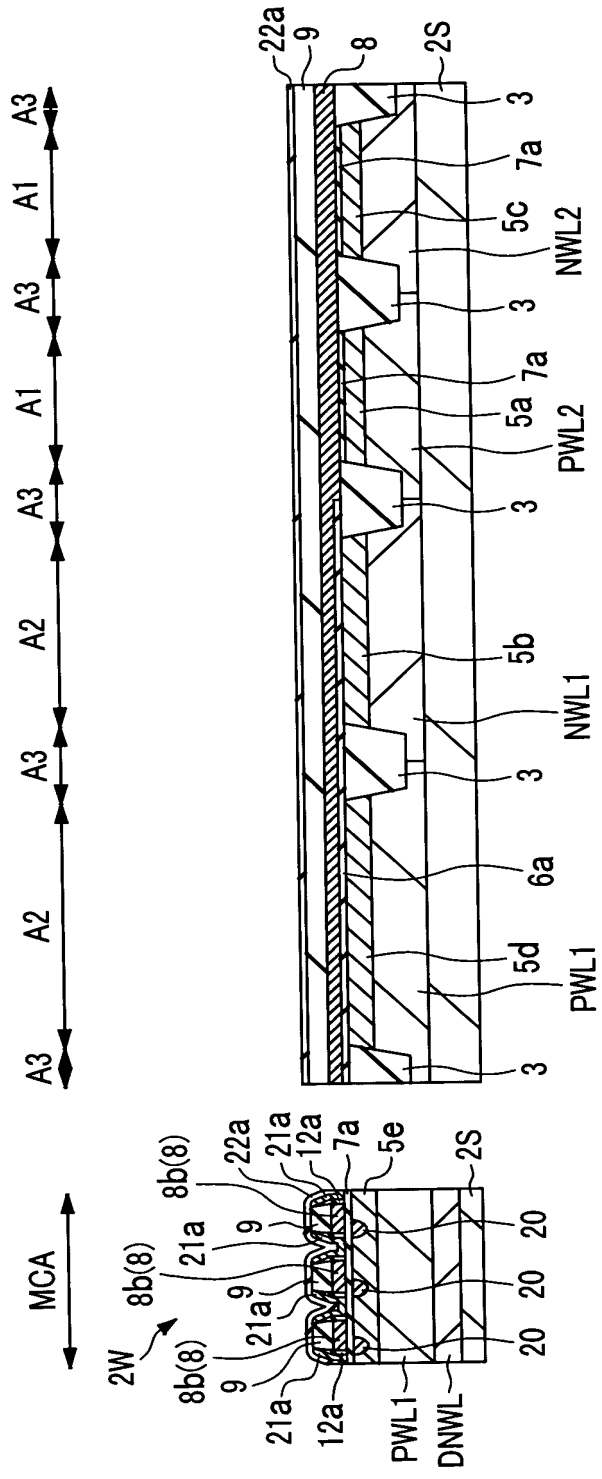
# FIG.34



# FIG. 35



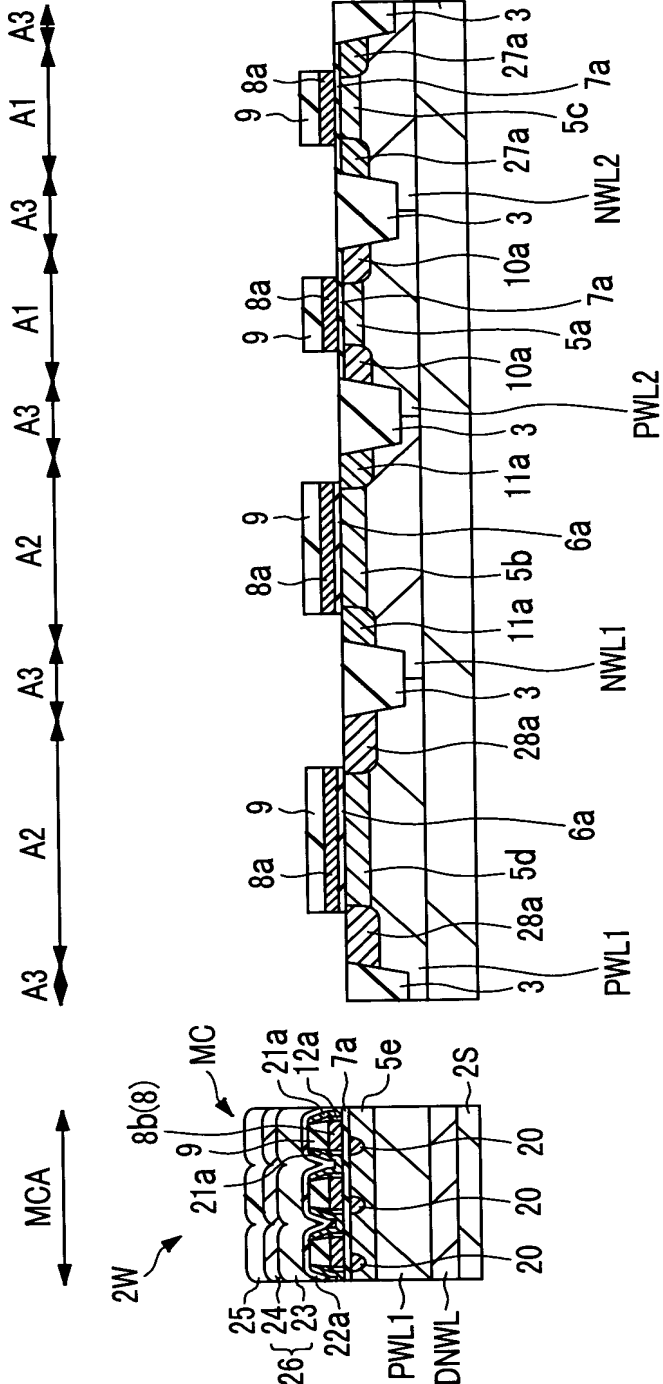
# FIG.36



• •



# F/G.38



**FIG. 39**

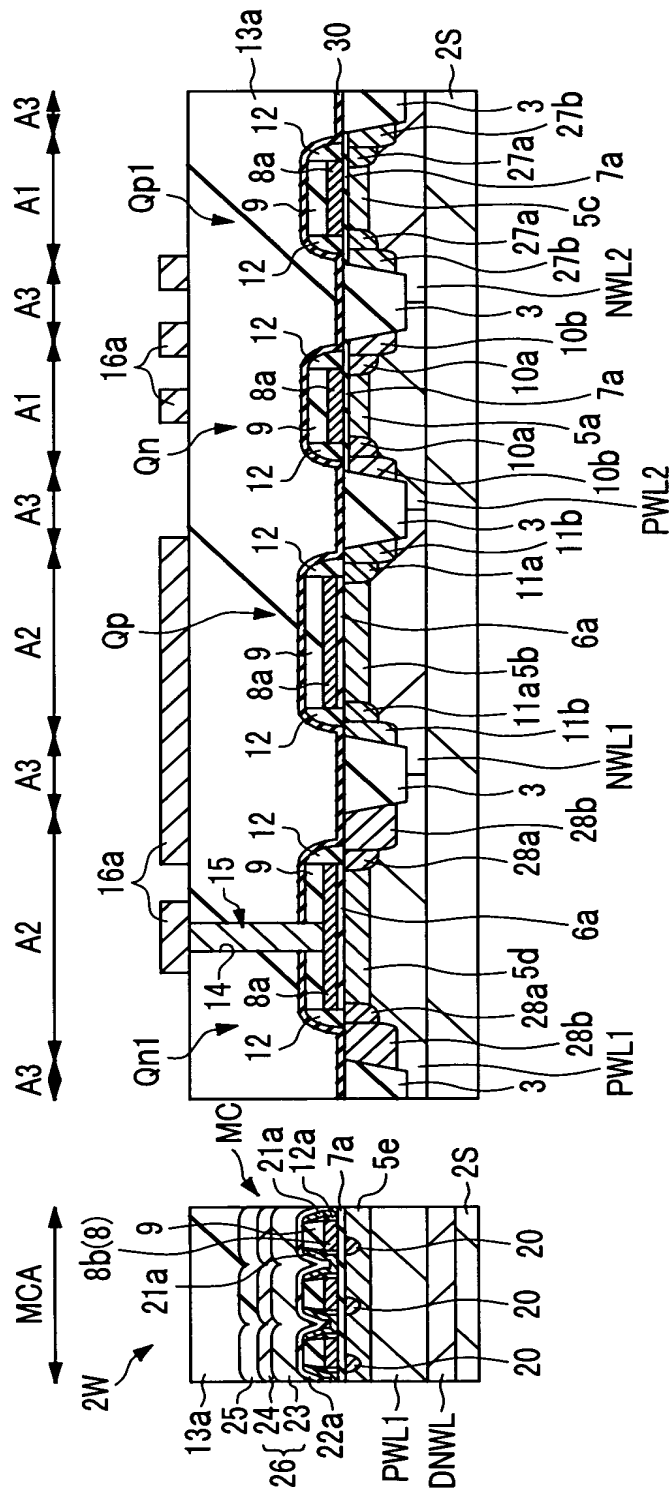


FIG.40

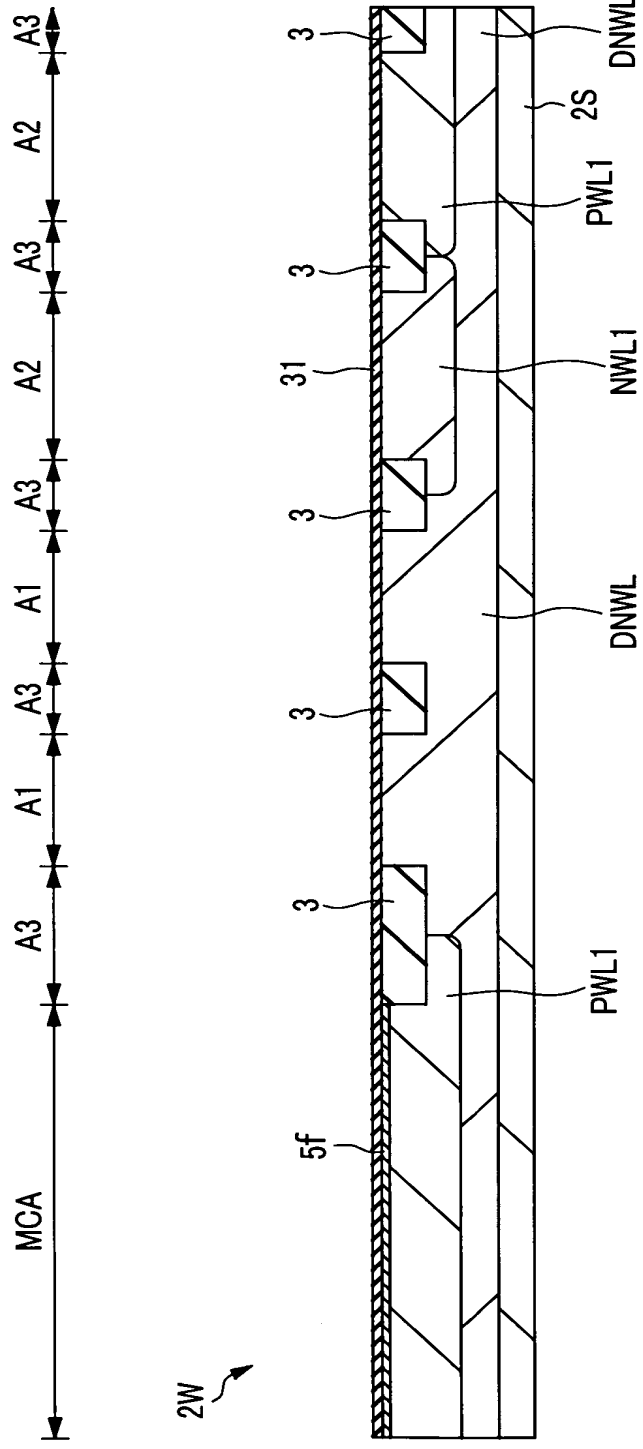
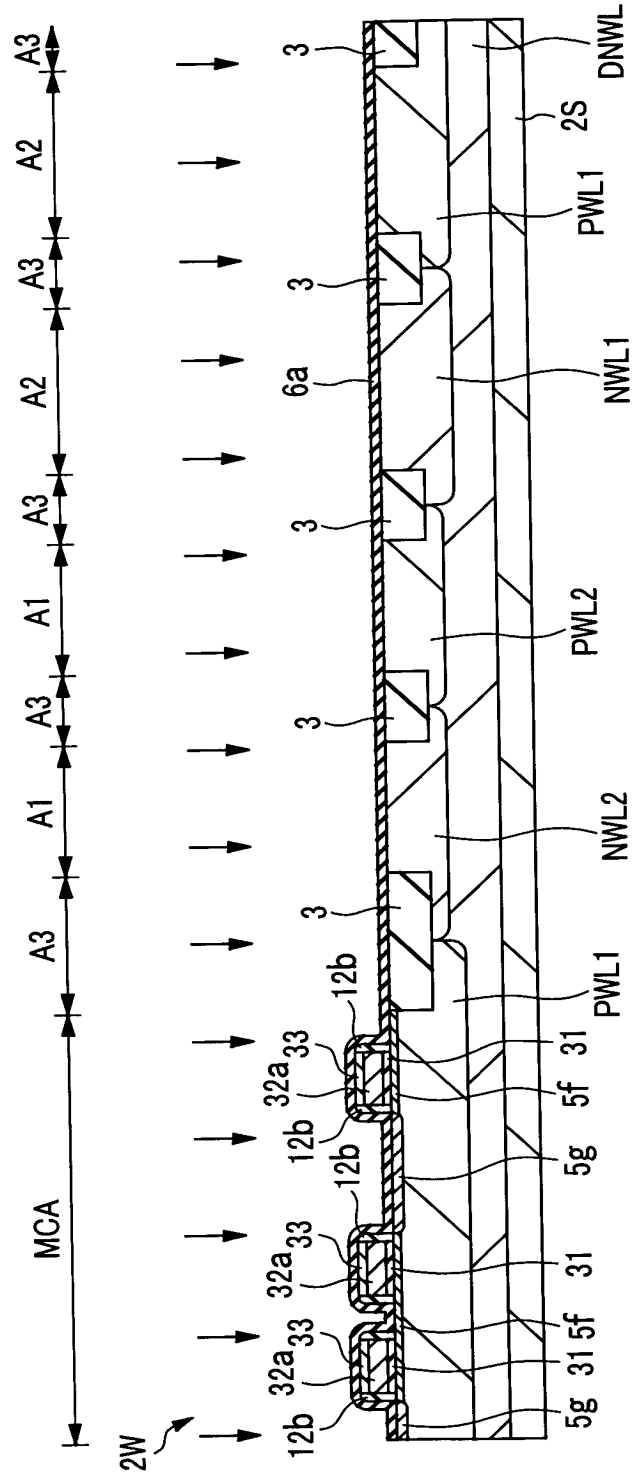
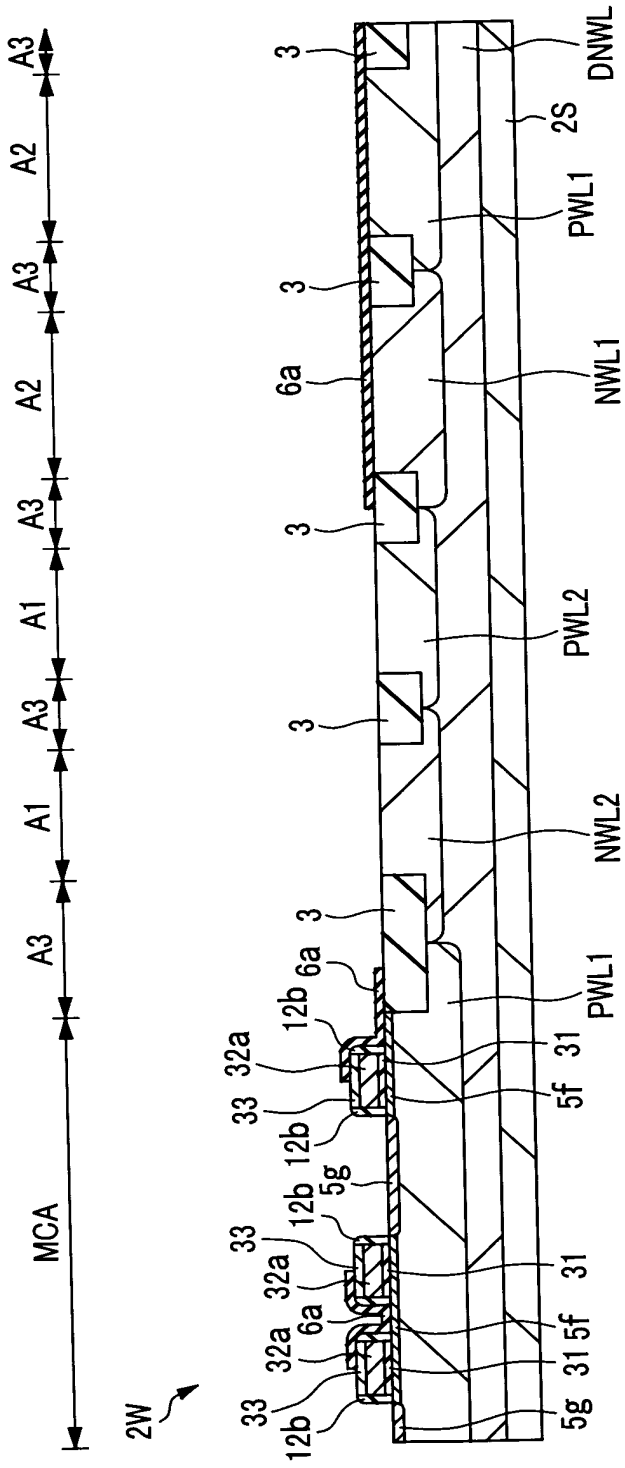


FIG.41

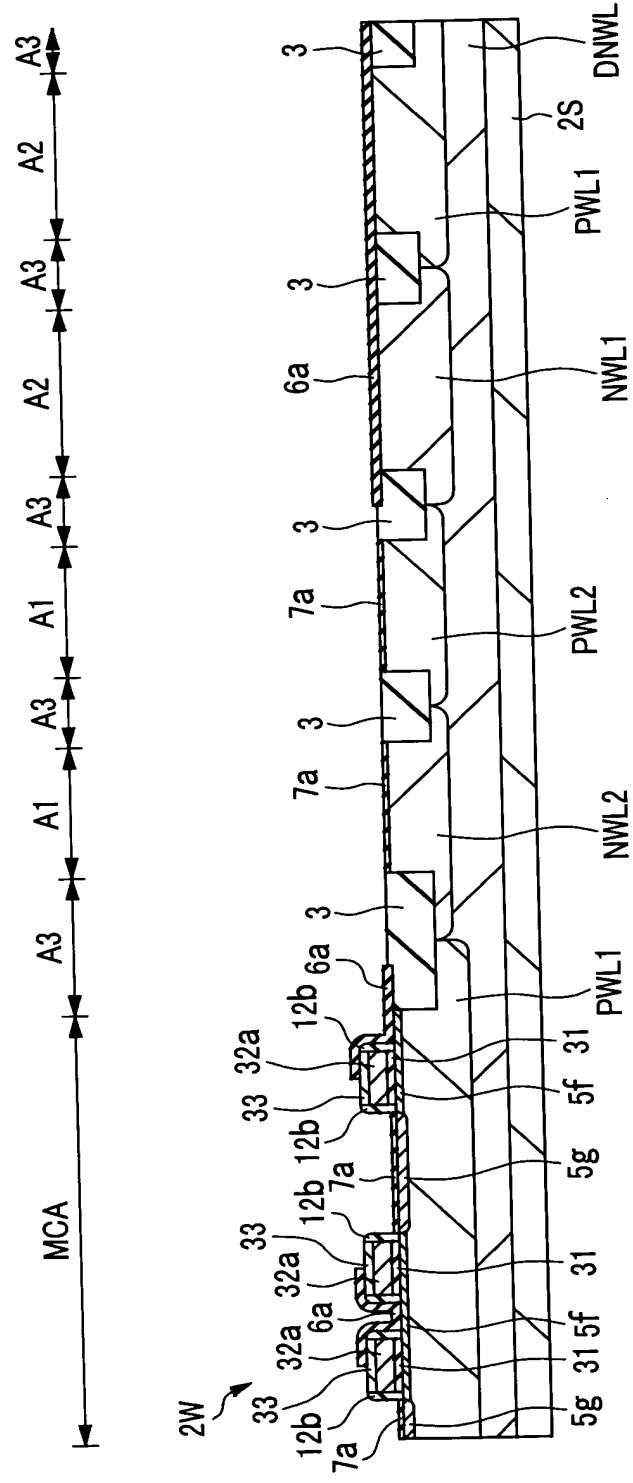




**FIG. 42**



# FIG.43



**FIG. 44**

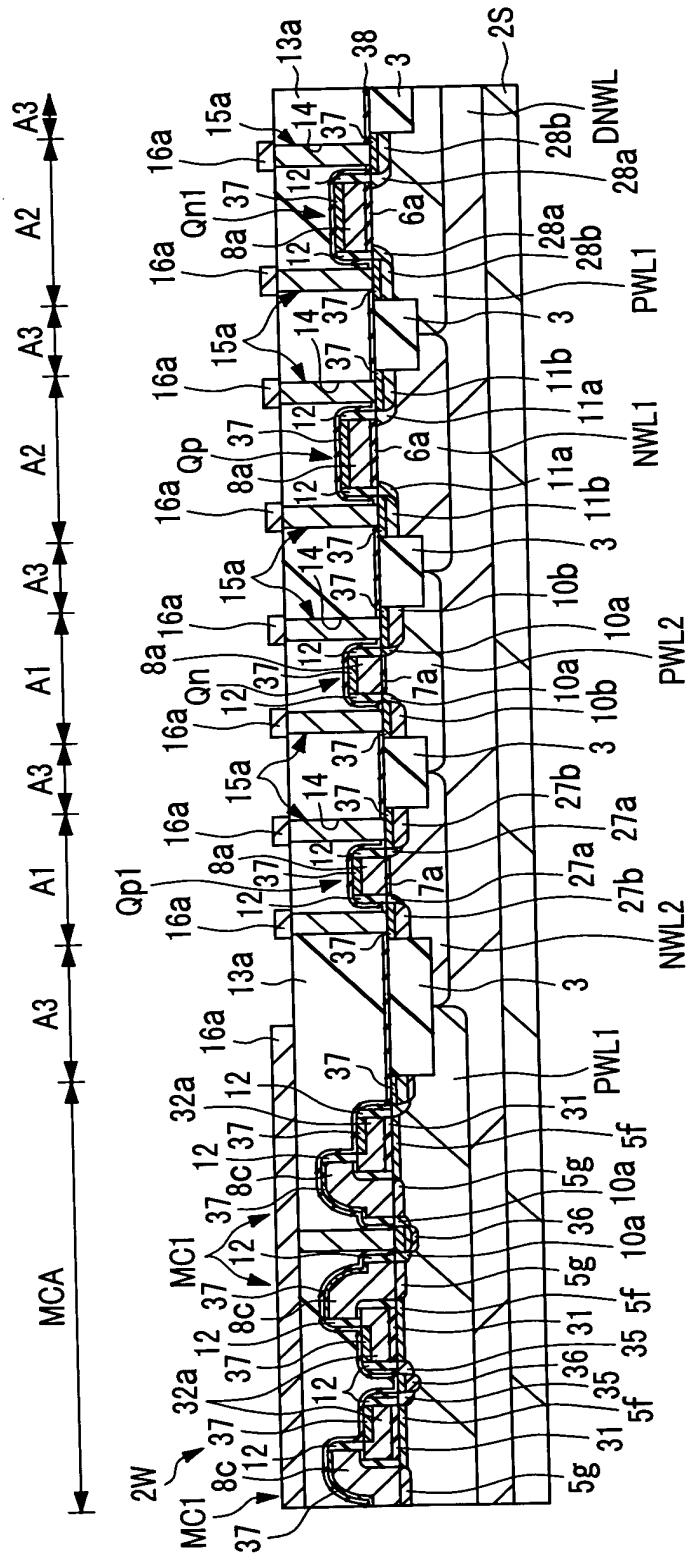
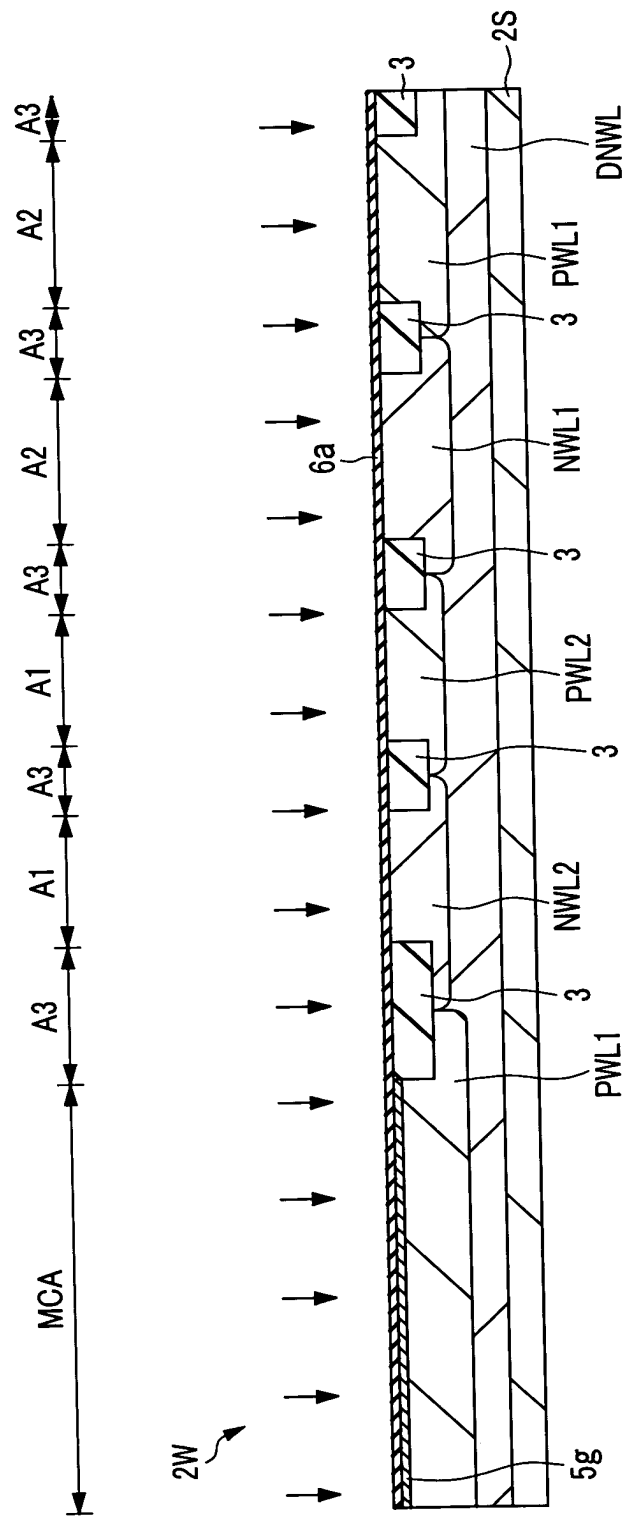
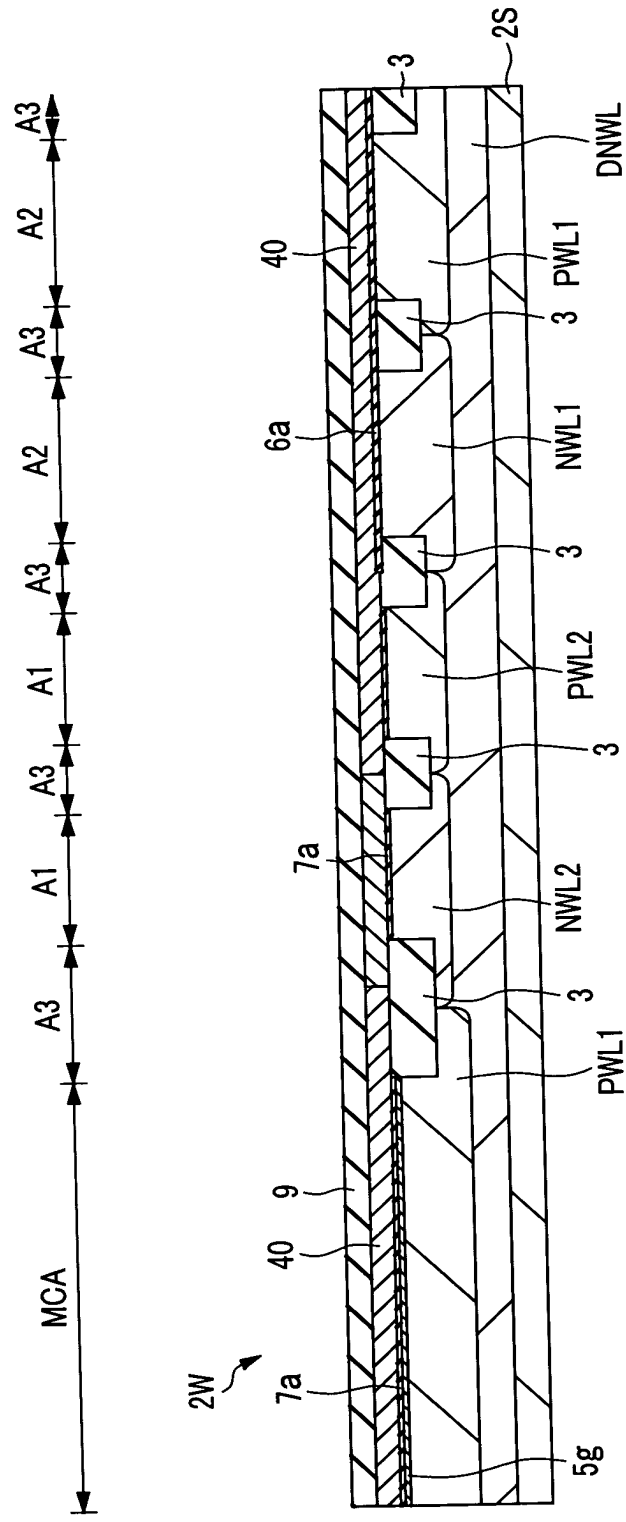


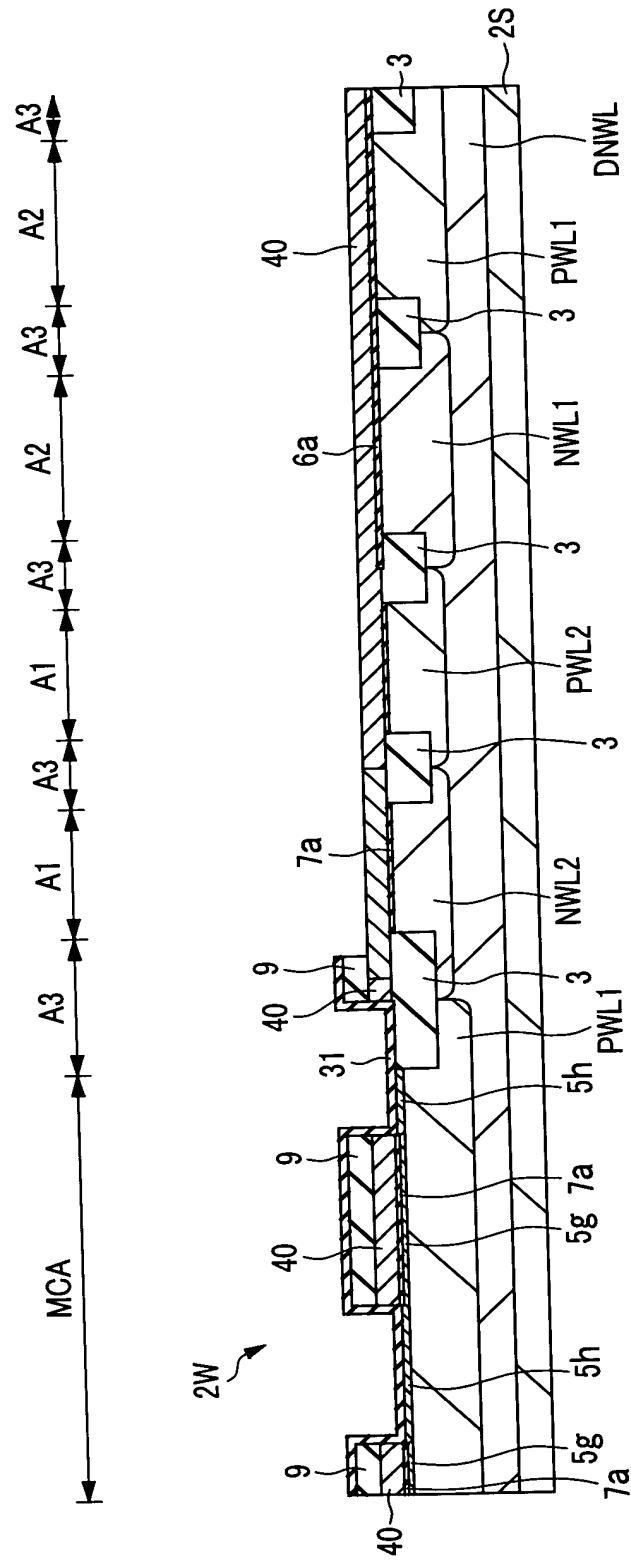
FIG.45



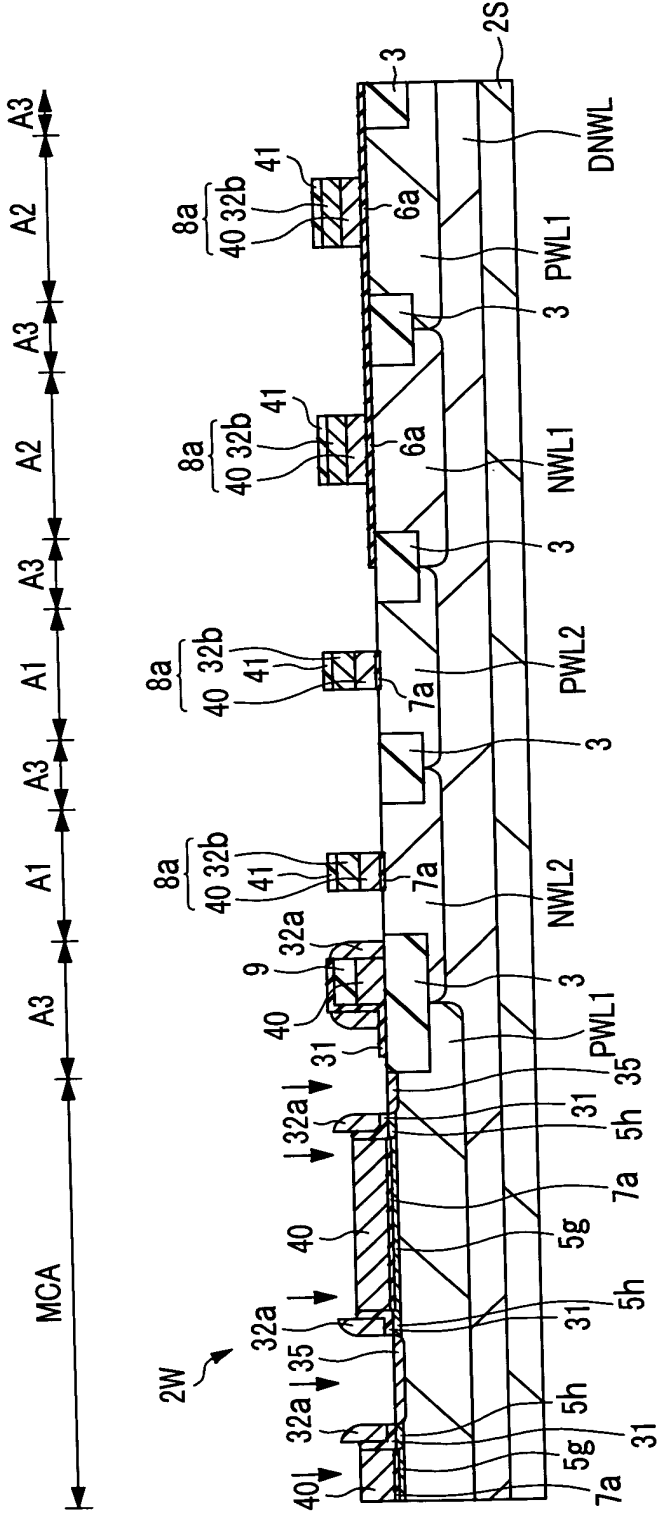
# FIG.46



**FIG. 47**



**FIG. 48**



**FIG. 49**

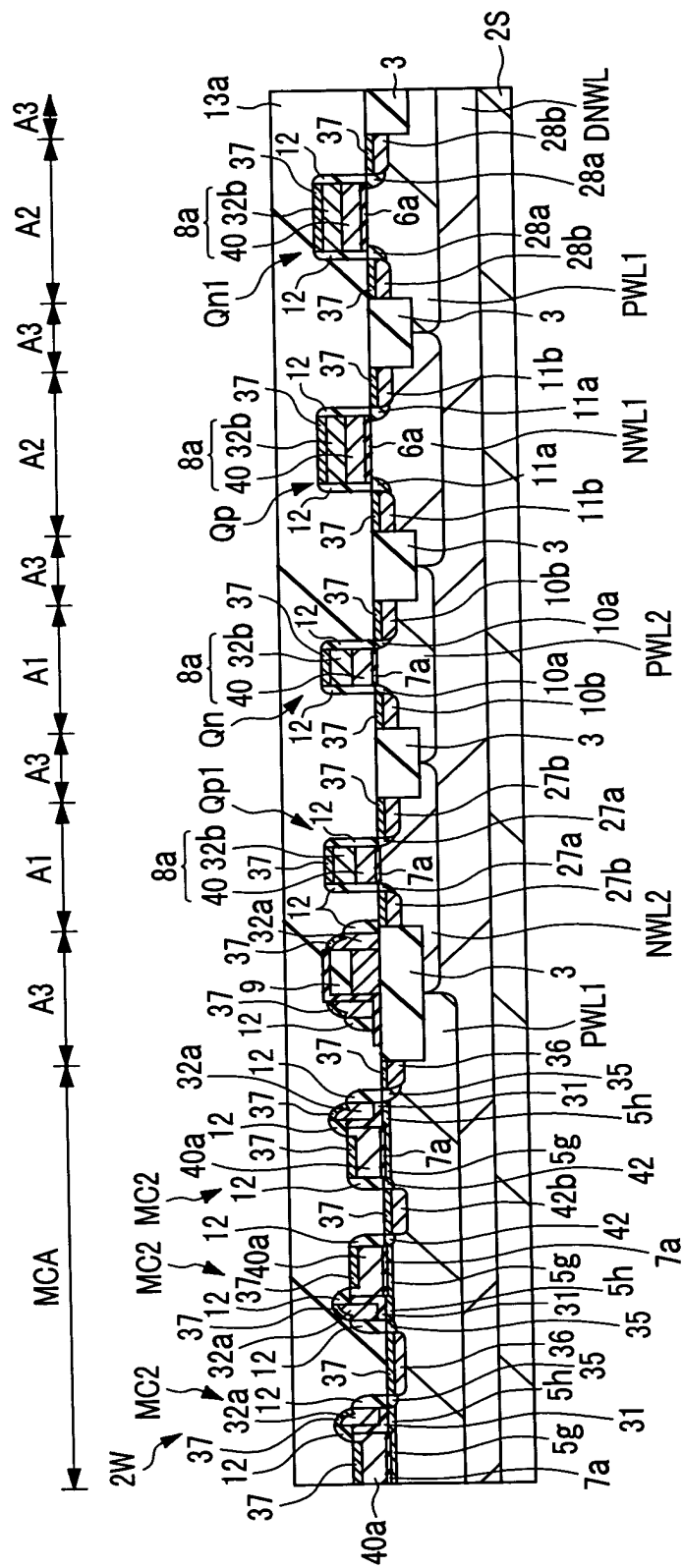




FIG.50

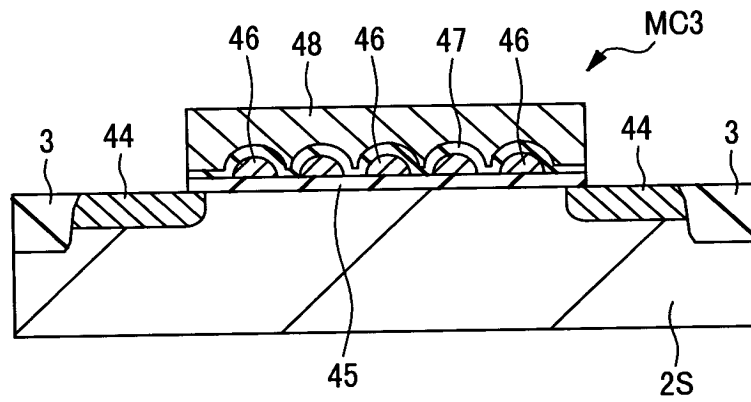
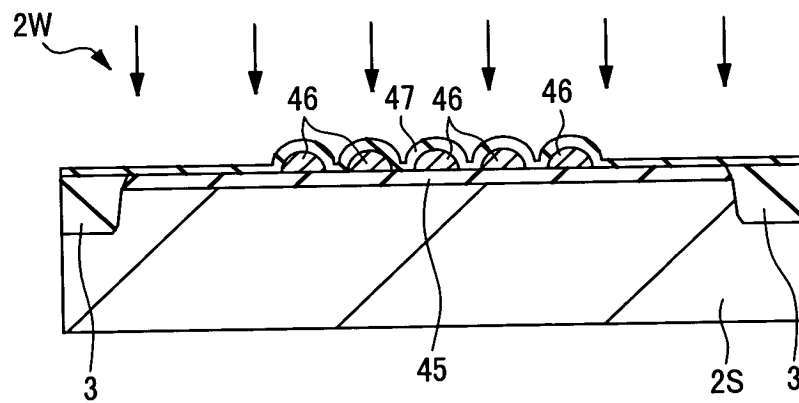
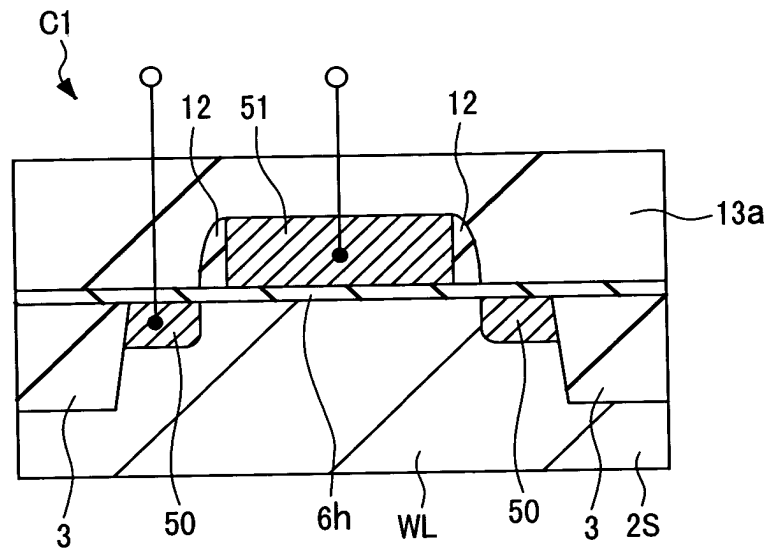


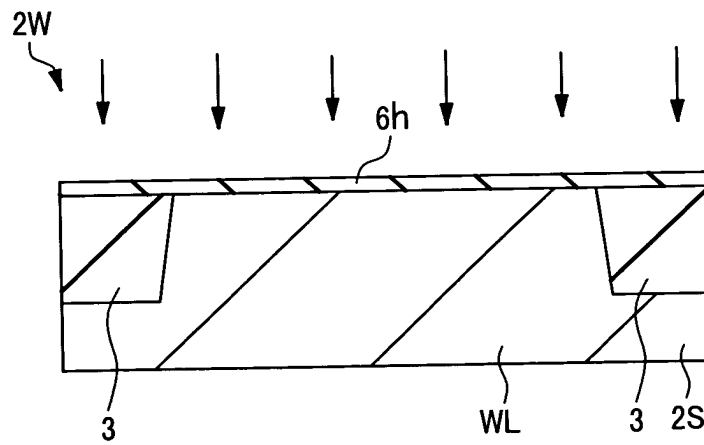
FIG.51



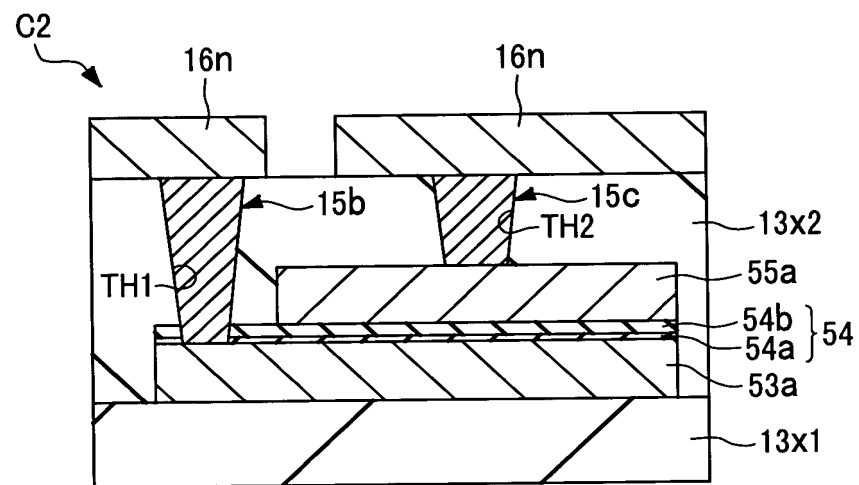
# FIG.52



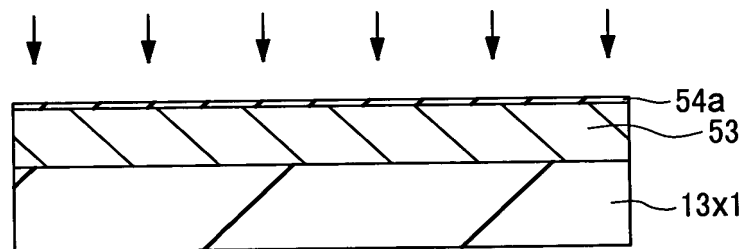
# FIG.53



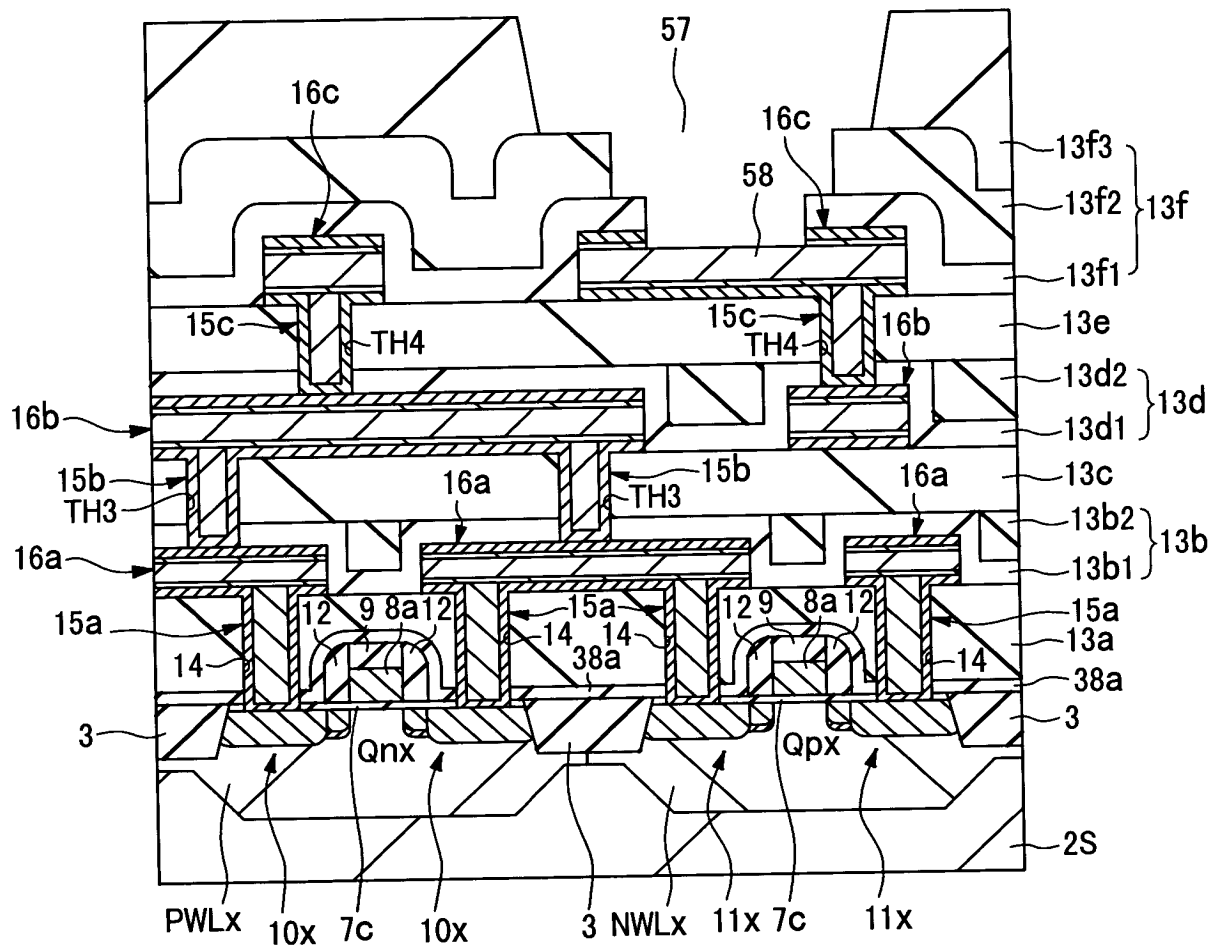
# FIG.54



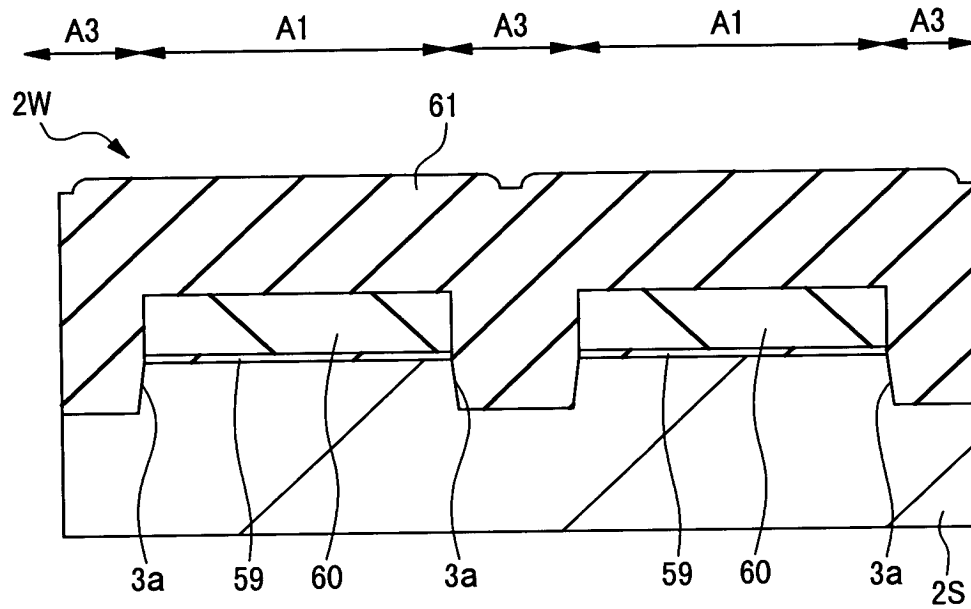
# FIG.55



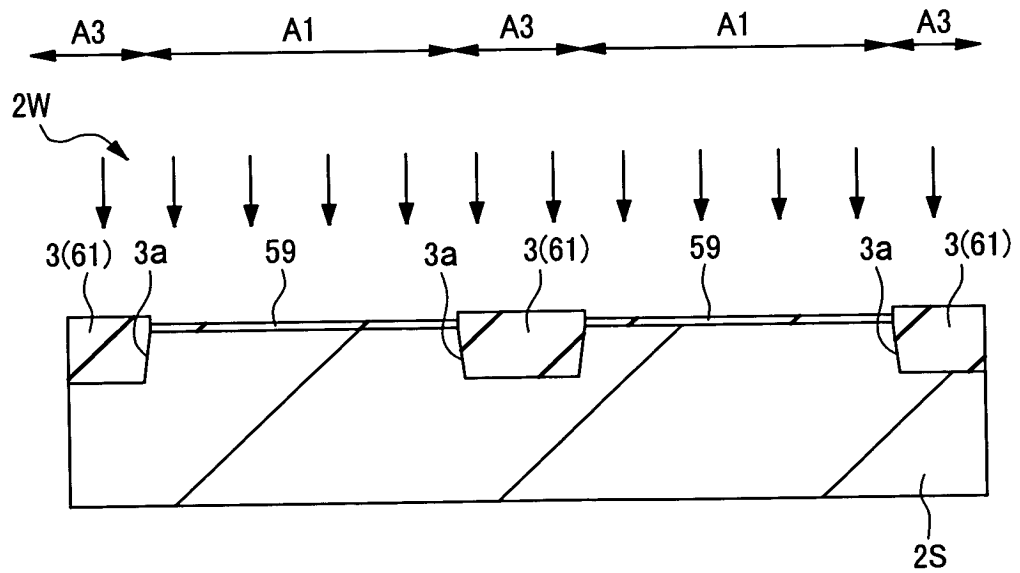
# FIG.56



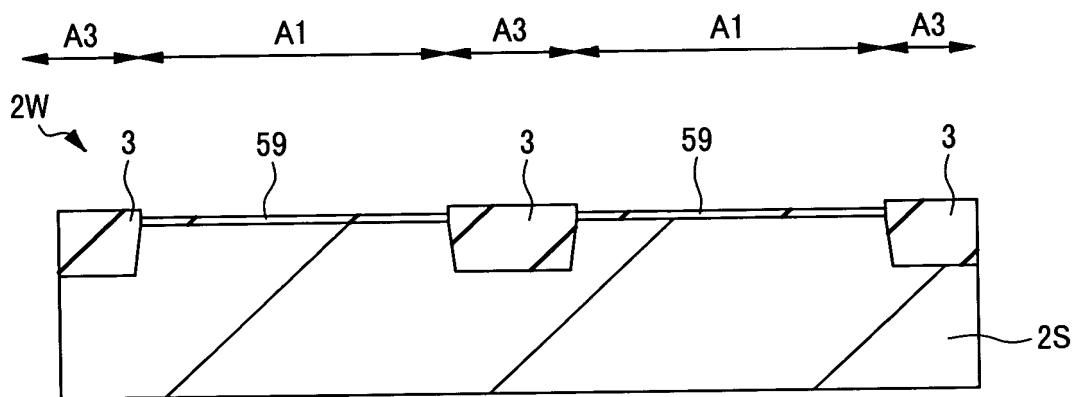
# FIG.57



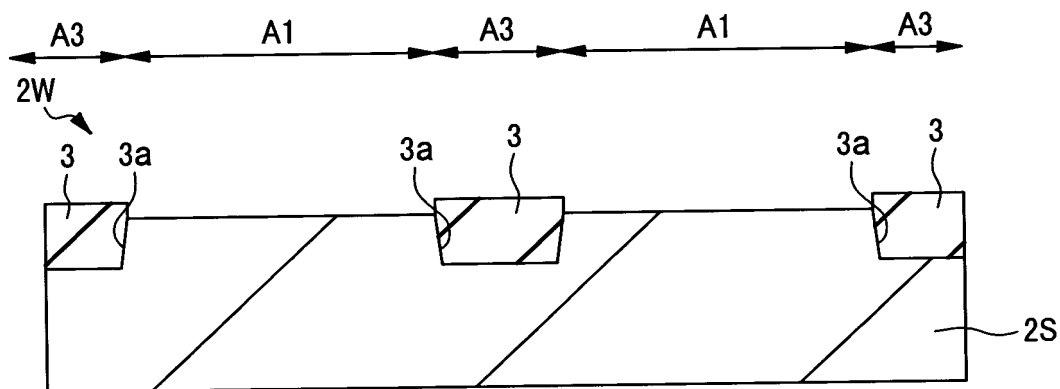
# FIG.58



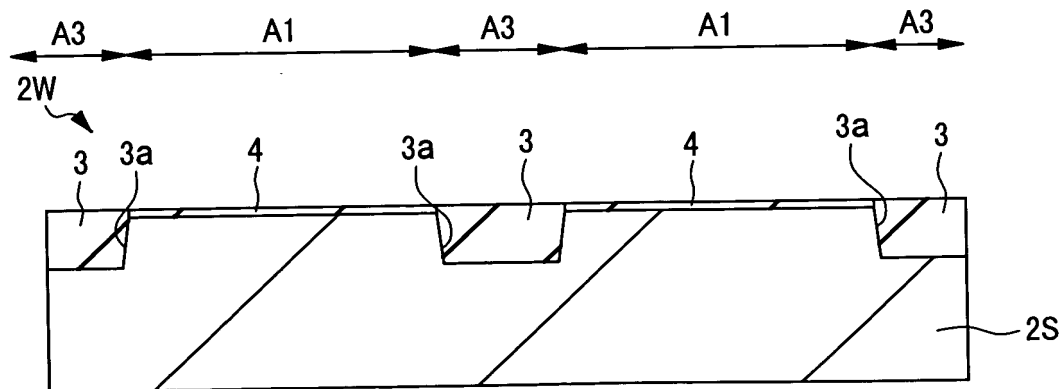
# FIG.59



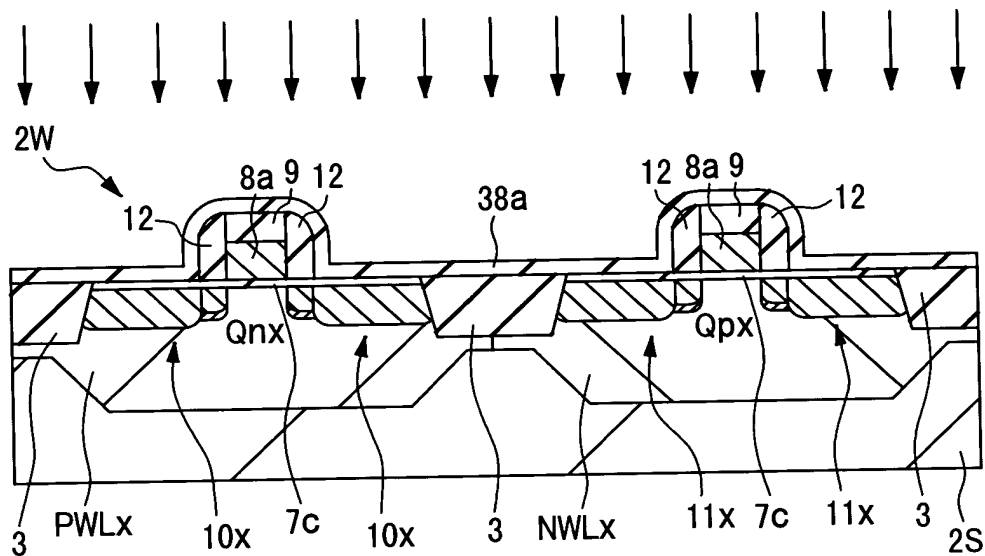
# FIG.60



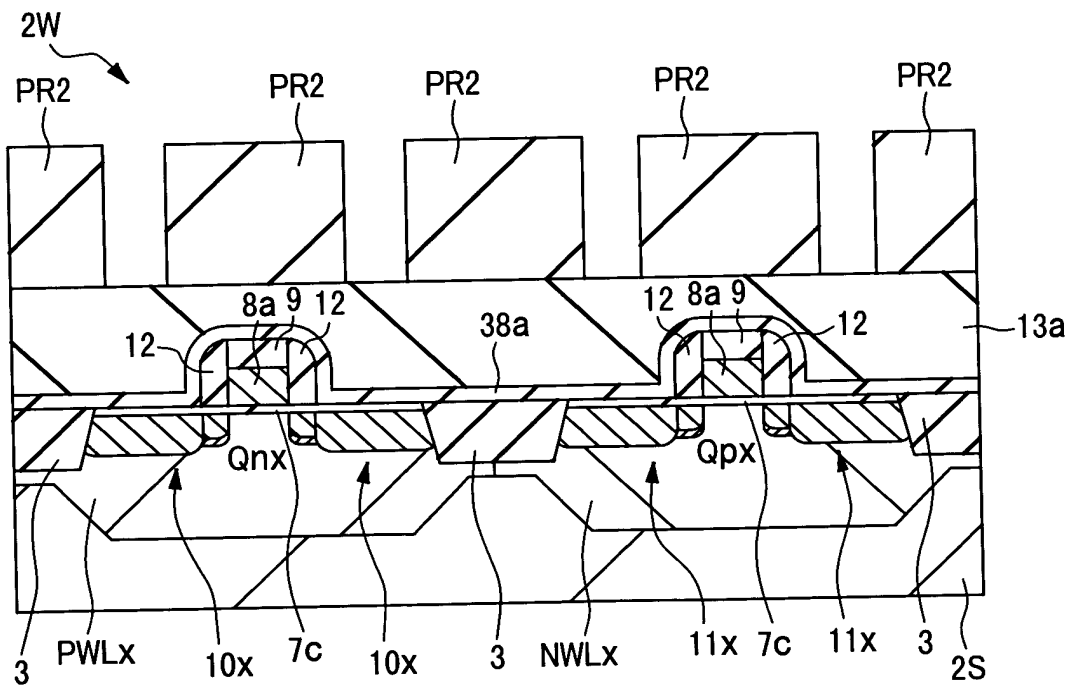
# FIG.61



# FIG.62



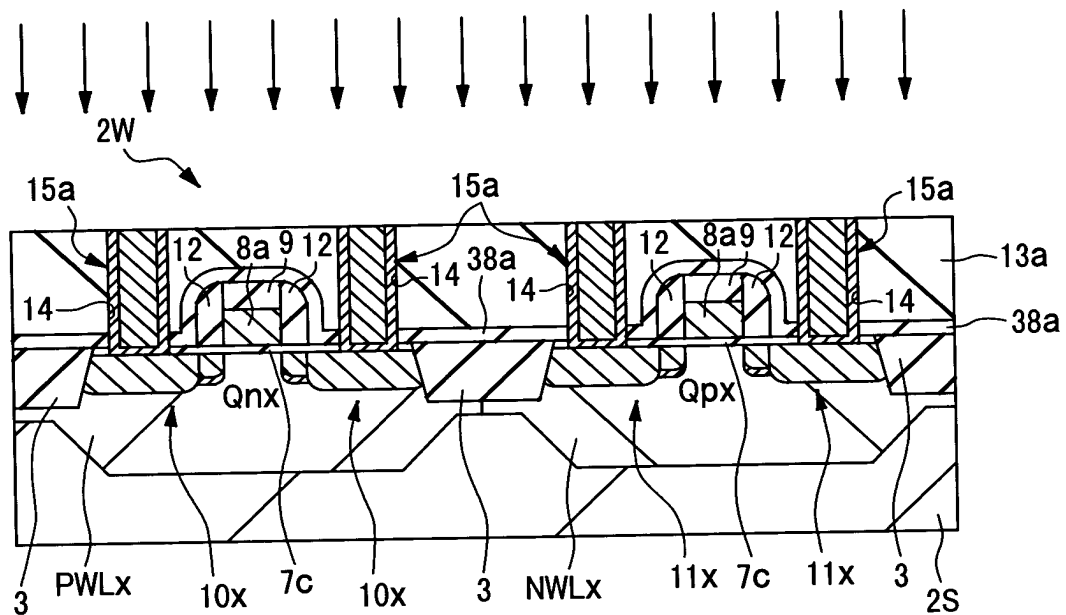
# FIG.63



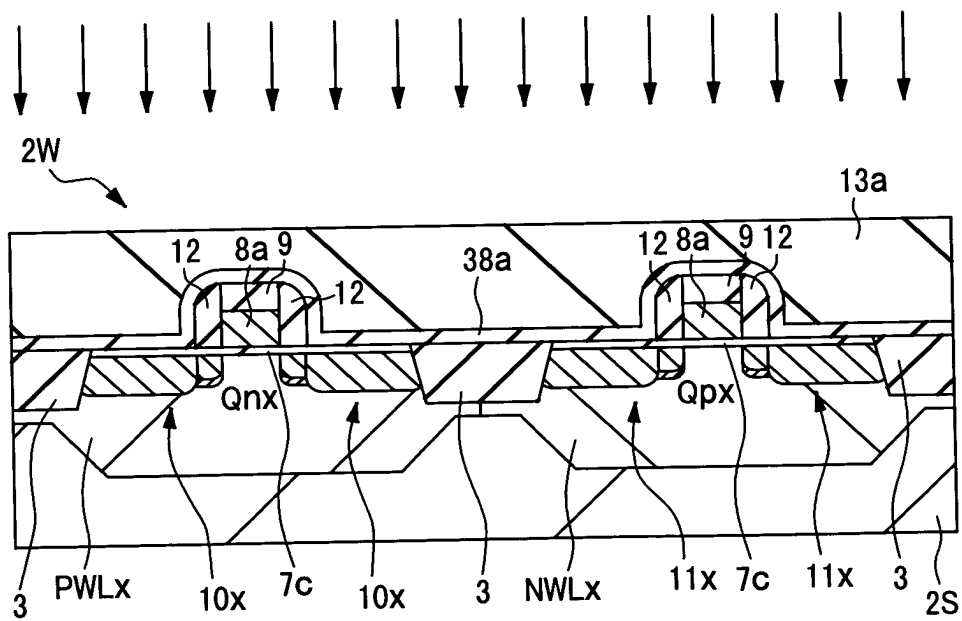




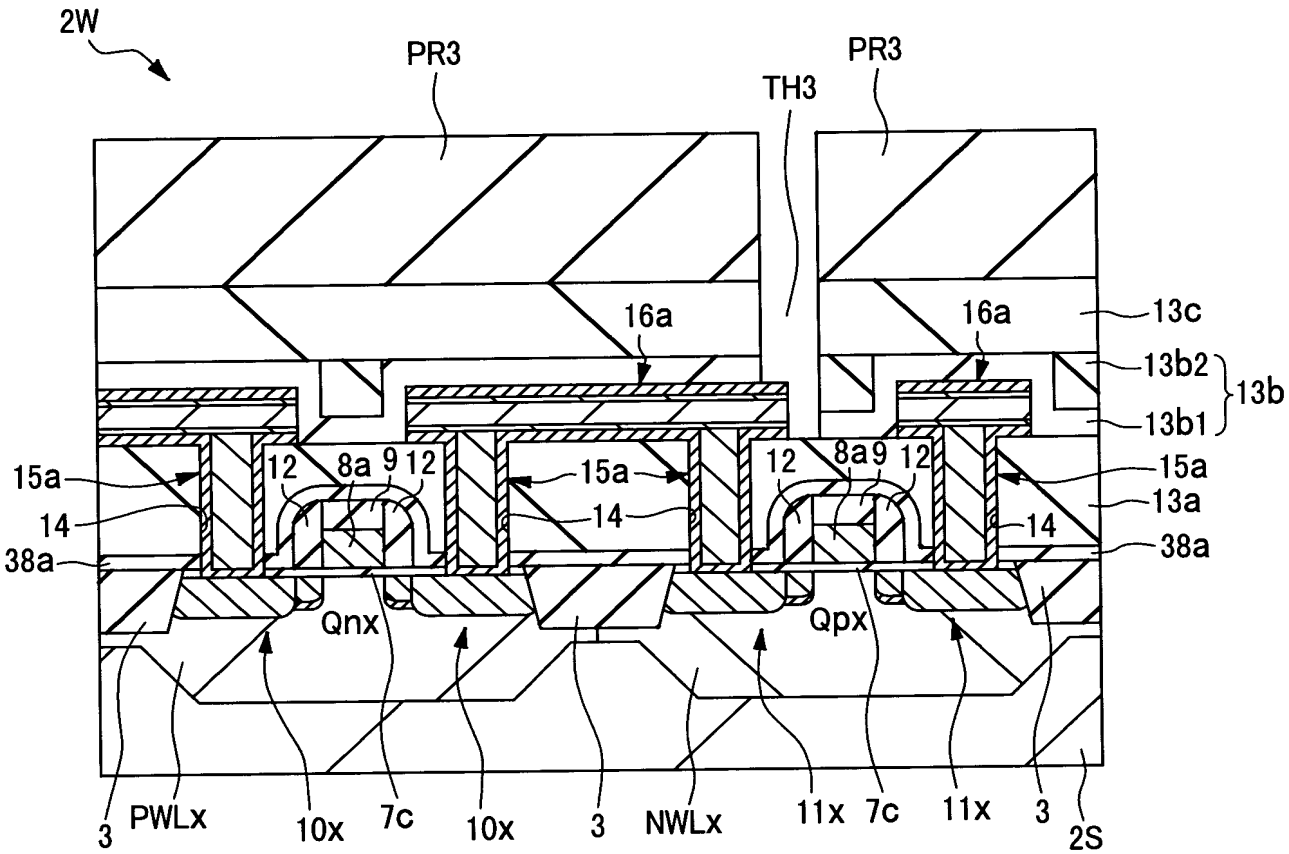
# FIG.66



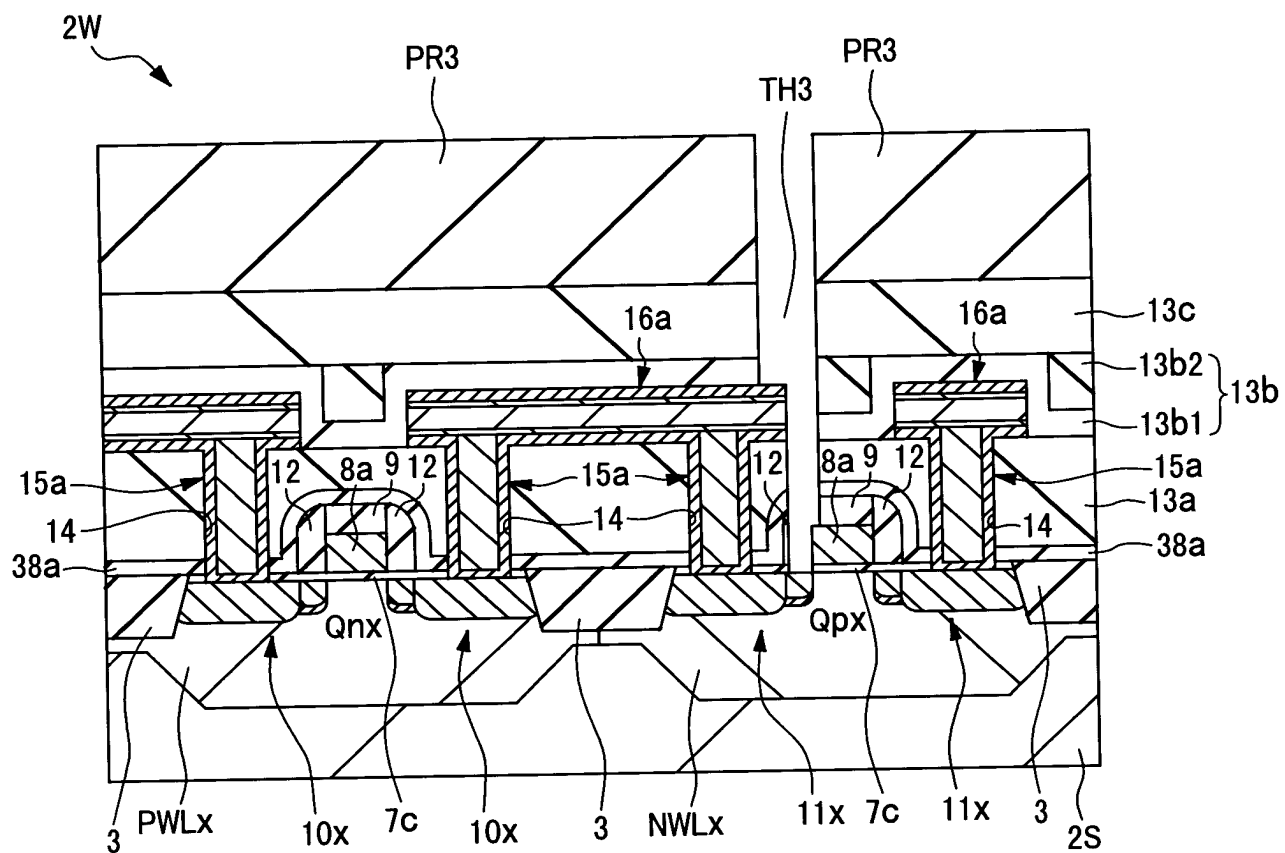
# FIG.67



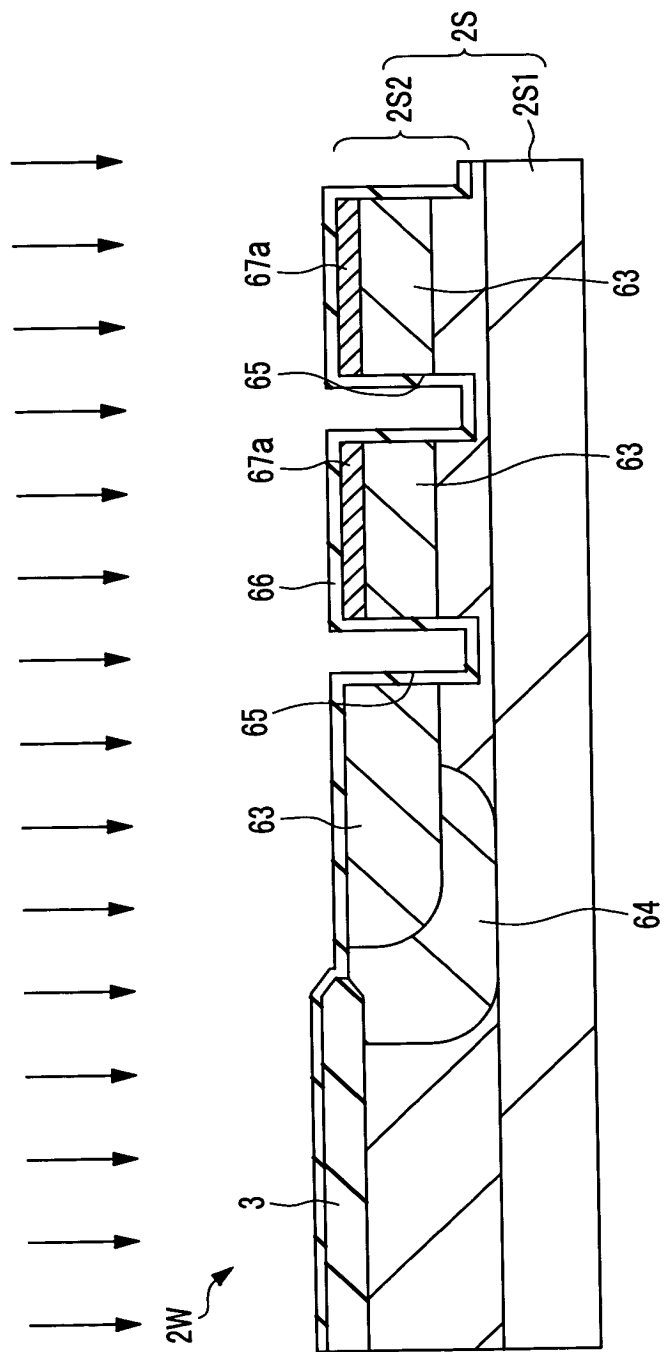
**FIG. 68**



# FIG.69



**FIG. 70**



# FIG. 71

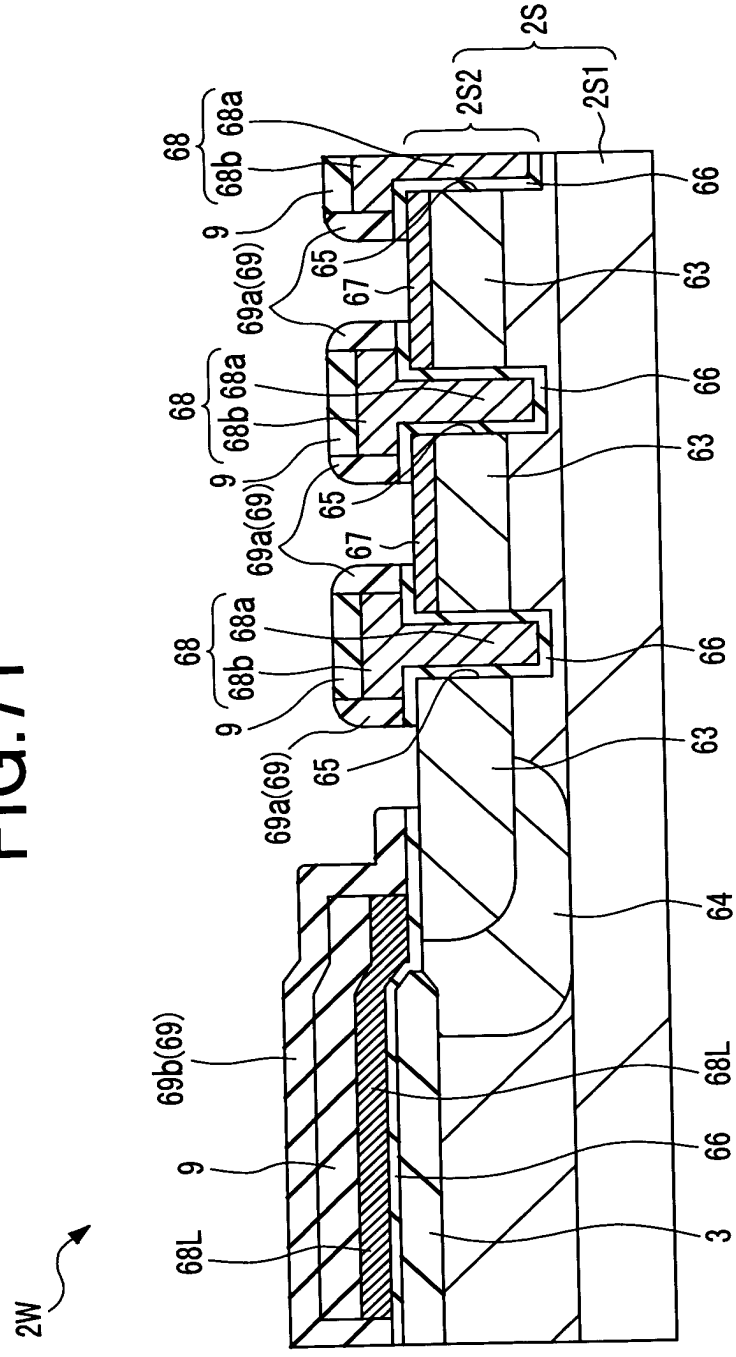


FIG.72

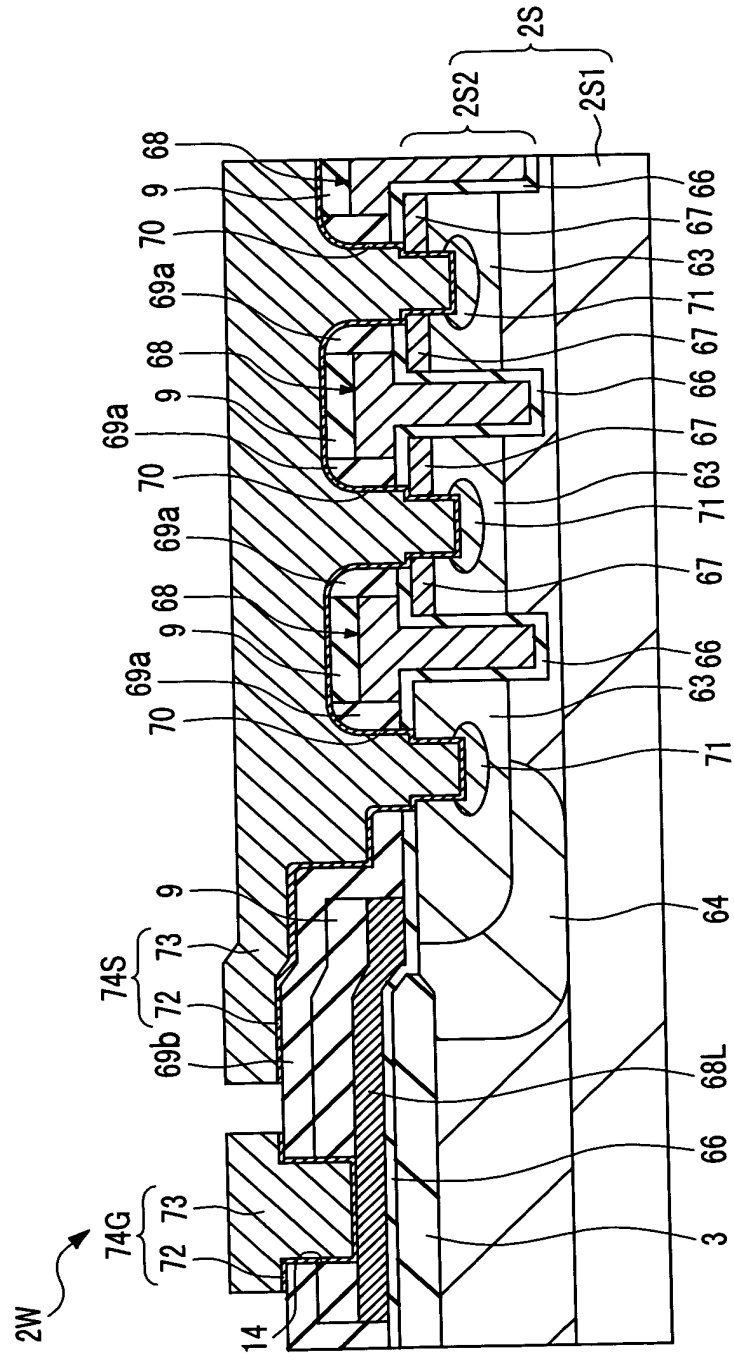


FIG.73

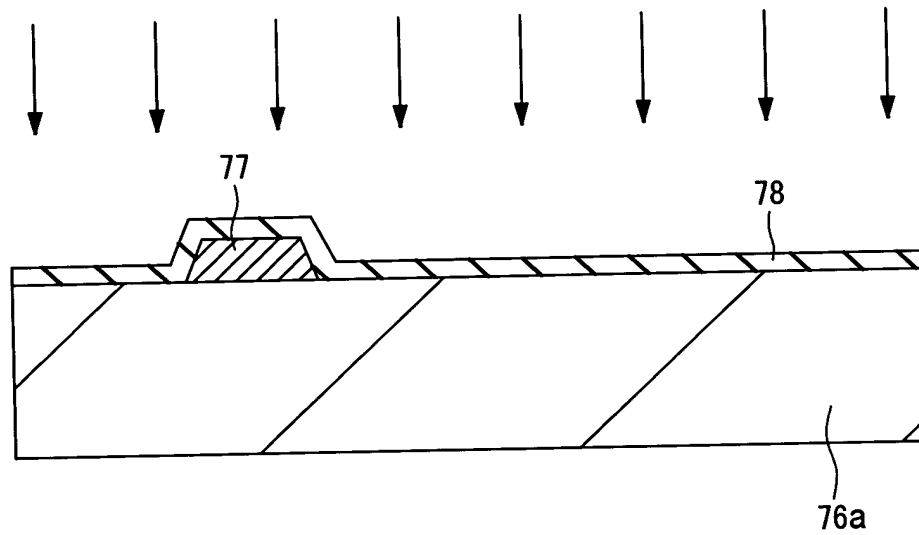


FIG.74

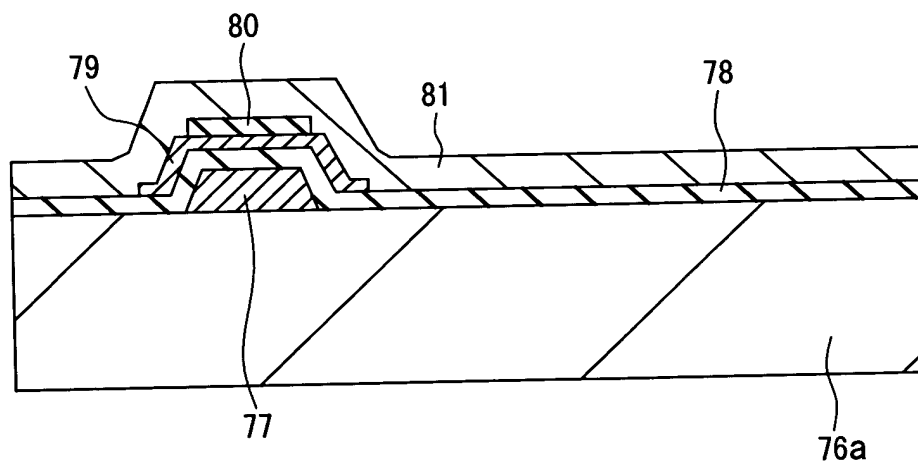


Figure 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 76a with a channel region 77 and a source/drain region 78. A gate structure is formed on the substrate, comprising a gate electrode 80, a gate insulating layer 81a, and a gate spacer 82. A gate contact 83 is also shown.



FIG.77

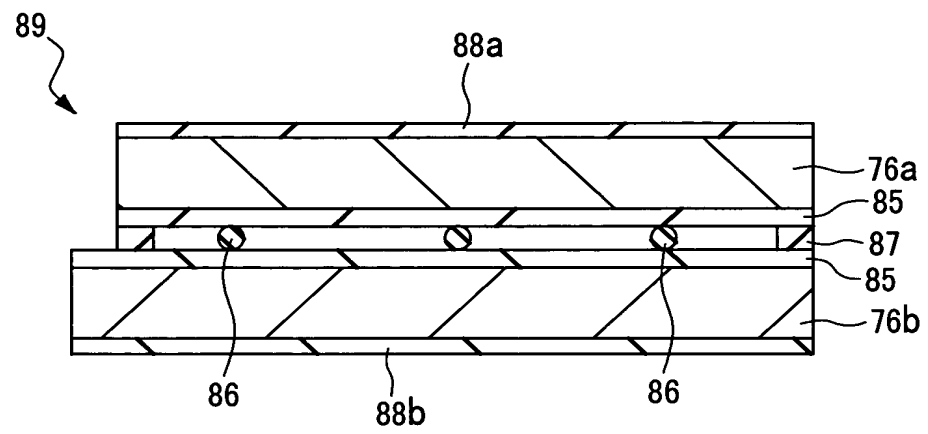


FIG.78

